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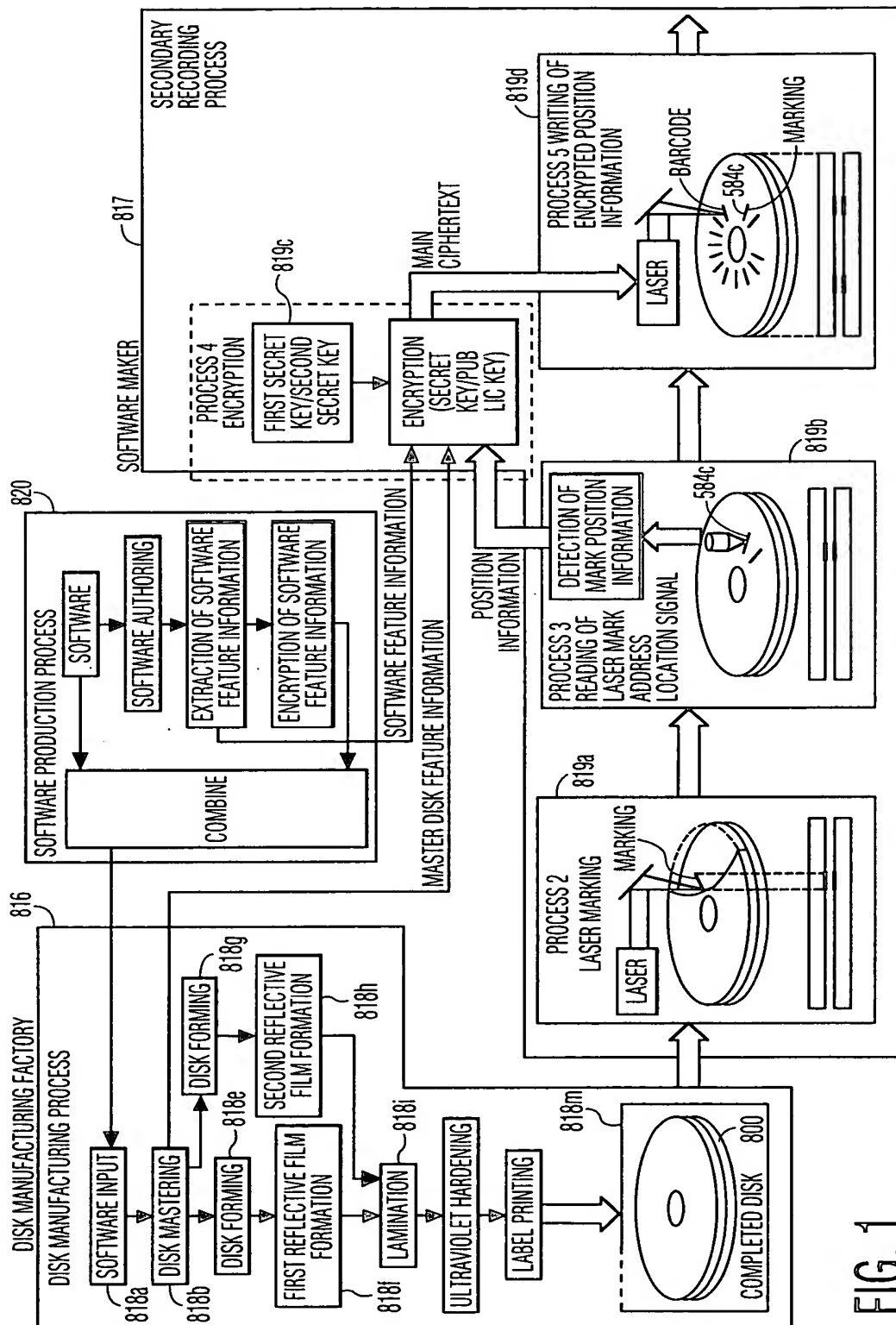
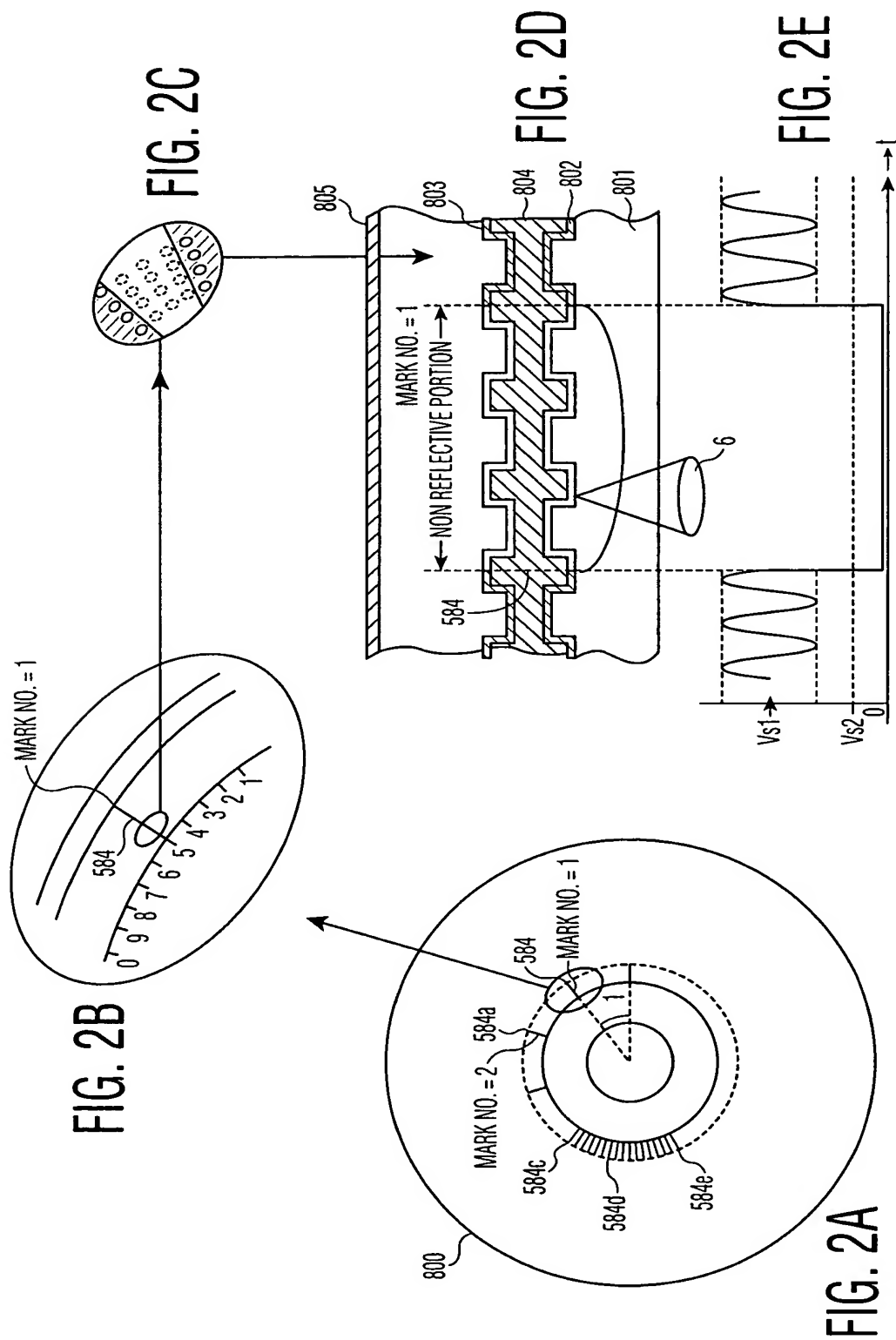


FIG. 1



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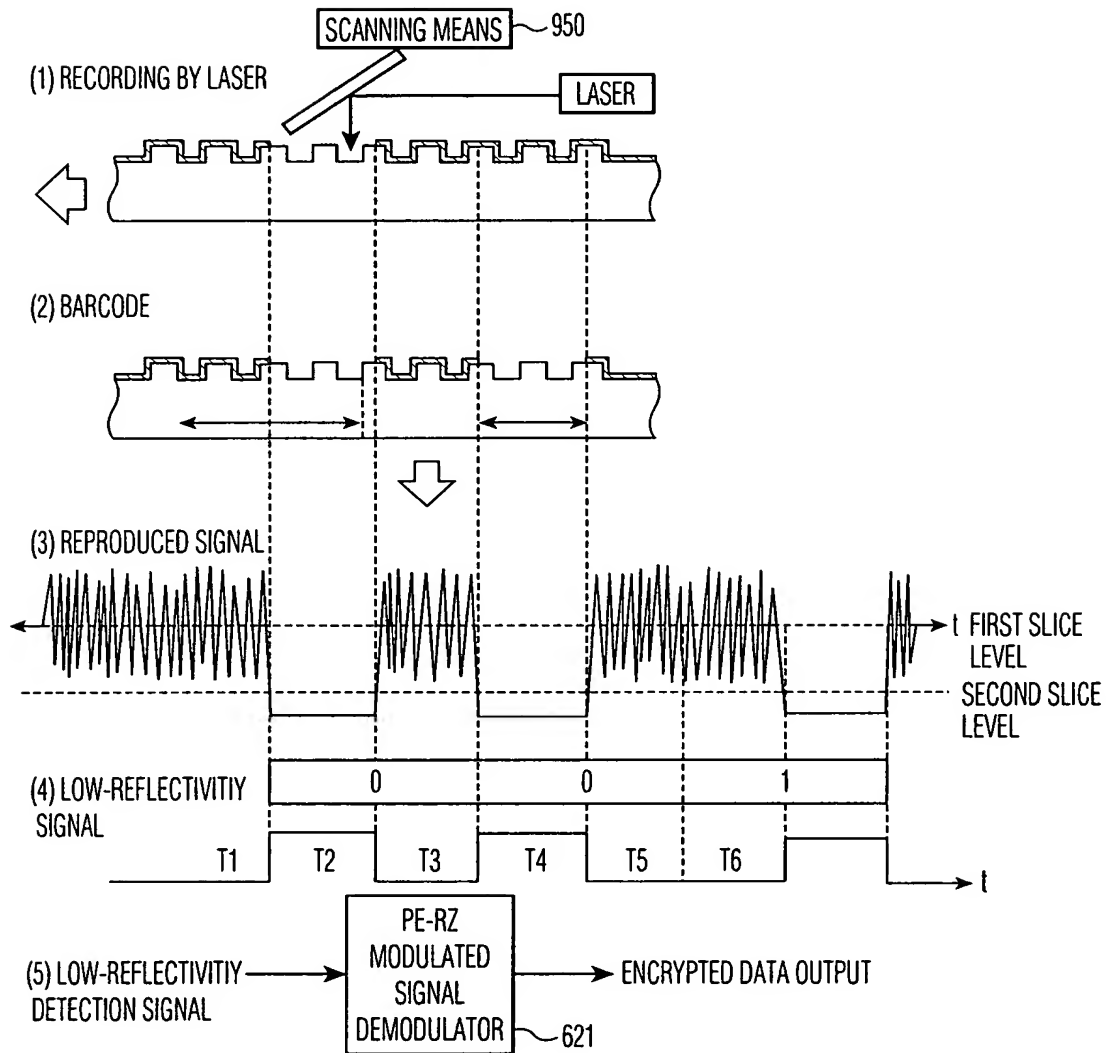
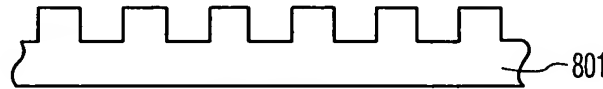


FIG. 3

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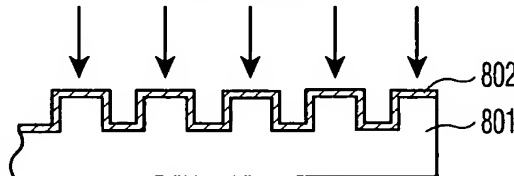
FIRST DISK FABRICATION PROCESS

STEP (1)  
FORMING



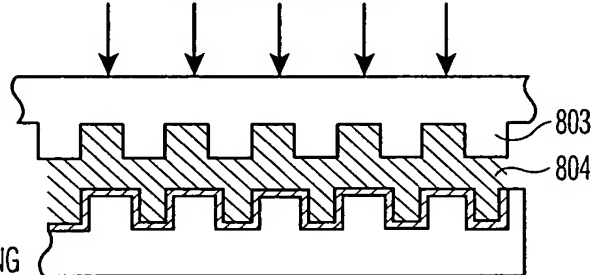
SPUTTERING

STEP (2)  
REFLECTIVE  
FILM FORMATION

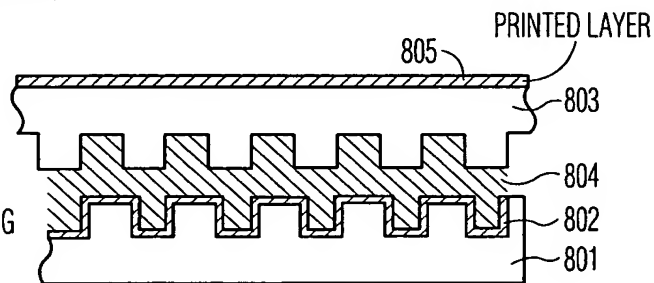


ULTRAVIOLET RADIATION

STEP (3)  
LAMINATION  
AND HARDENING

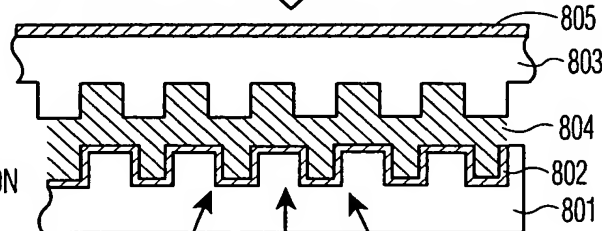


STEP (4)  
LABEL PRINTING



SECONDARY  
RECORDING  
PROCESS

STEP (5)  
FORMATION  
OF FIRST  
OPTICAL  
MARK



PULSED LASER 813



FIG. 4

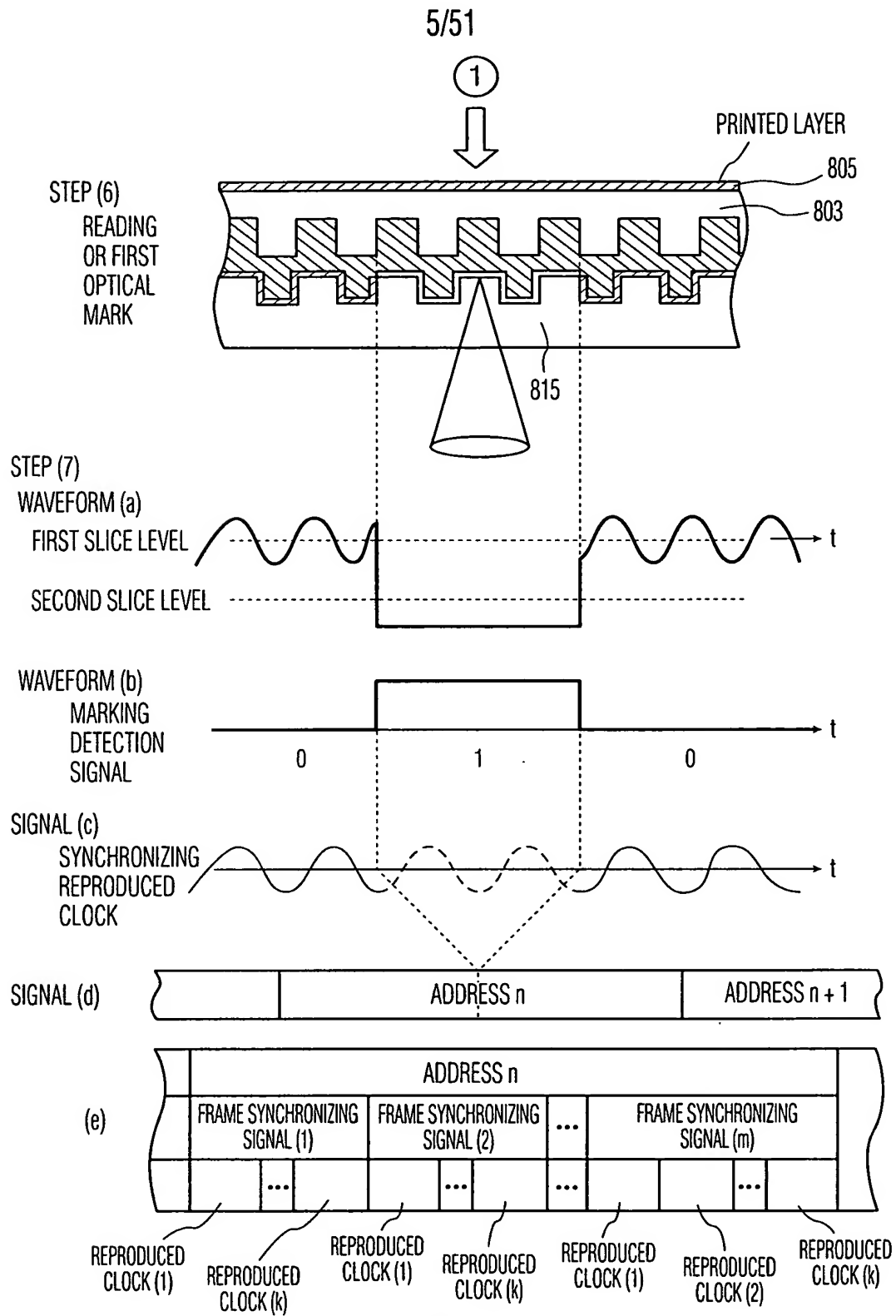


FIG. 5

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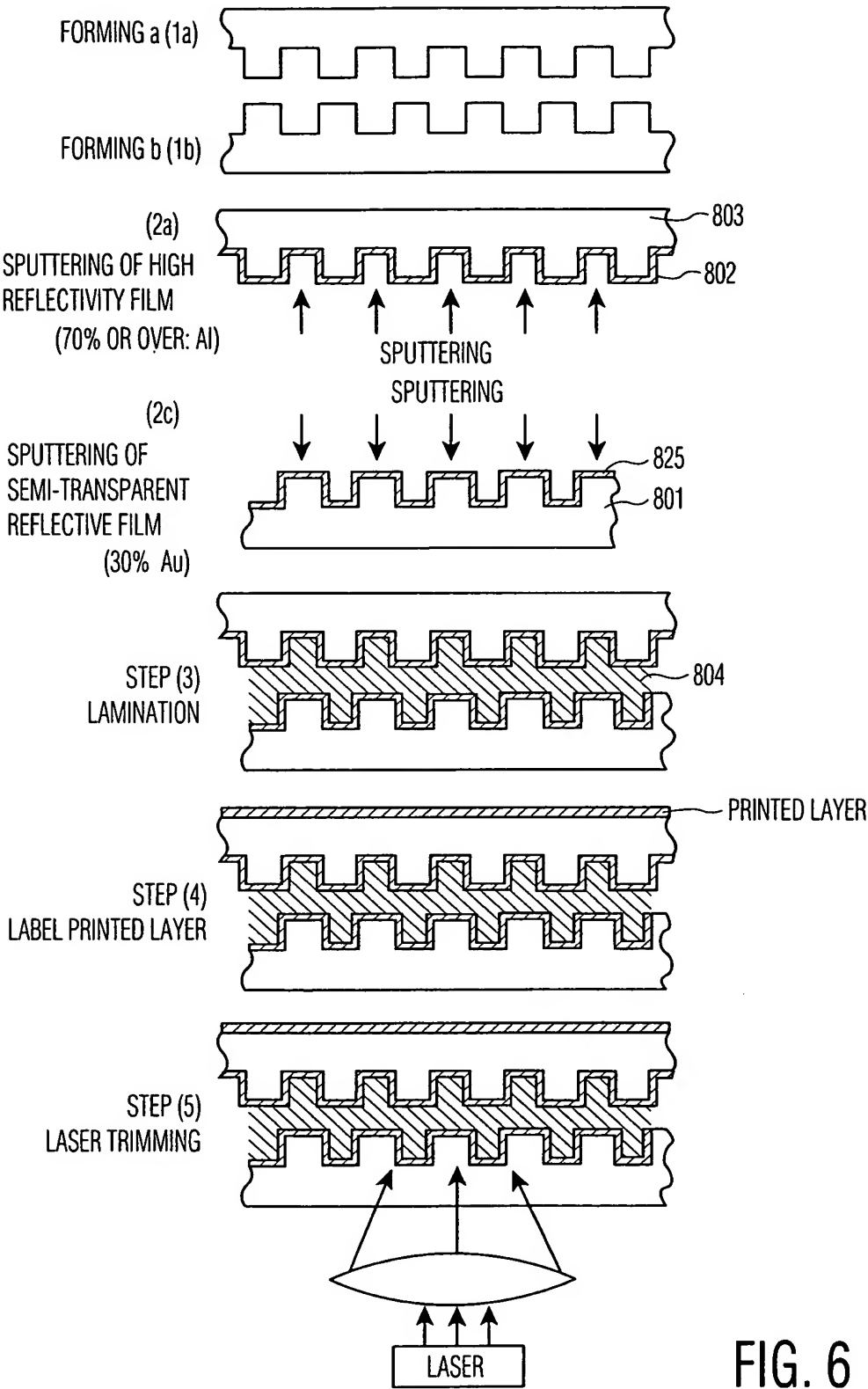
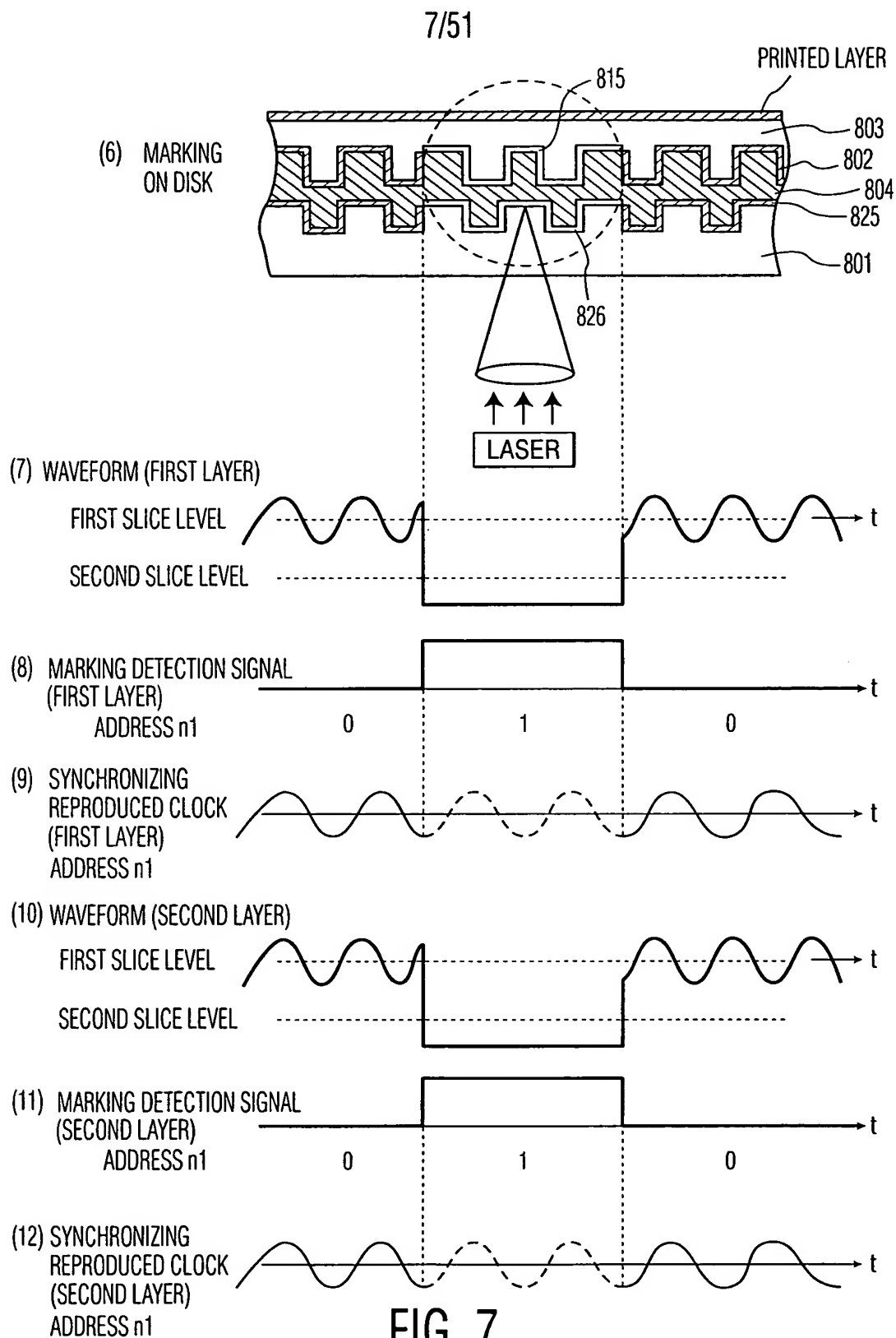


FIG. 6



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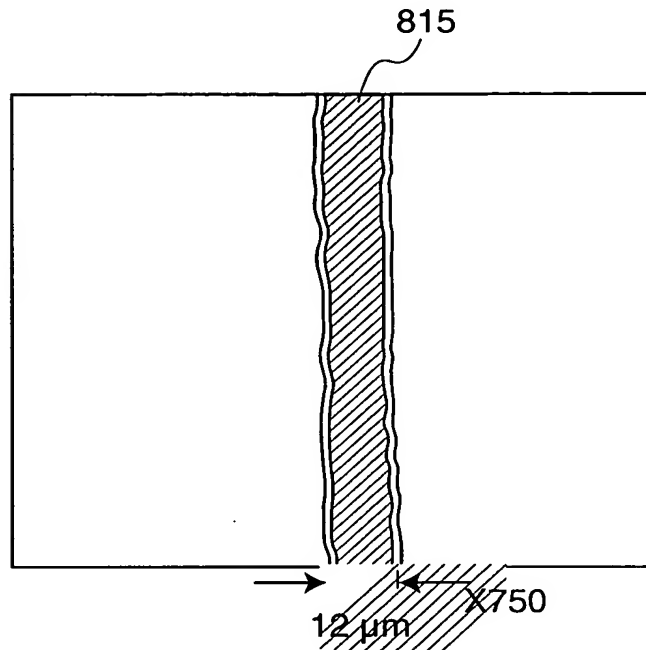


FIG. 51

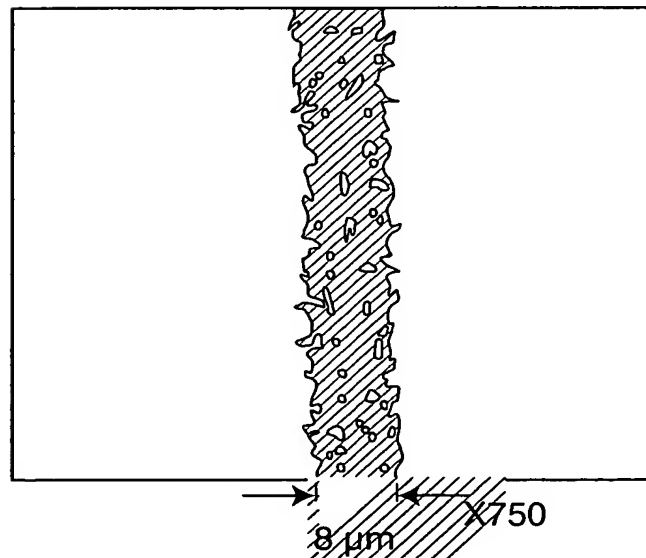


FIG. 52



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FIG. 9A

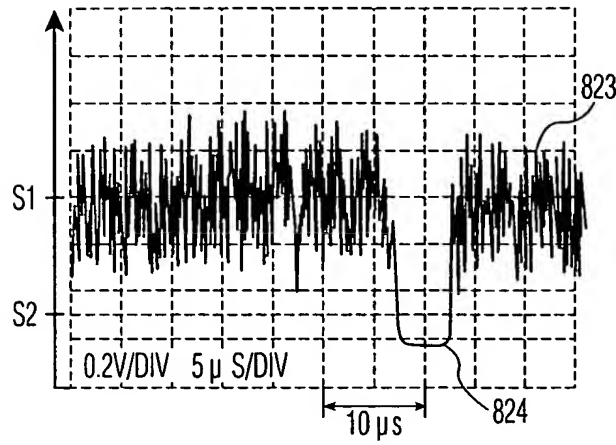


FIG. 9B

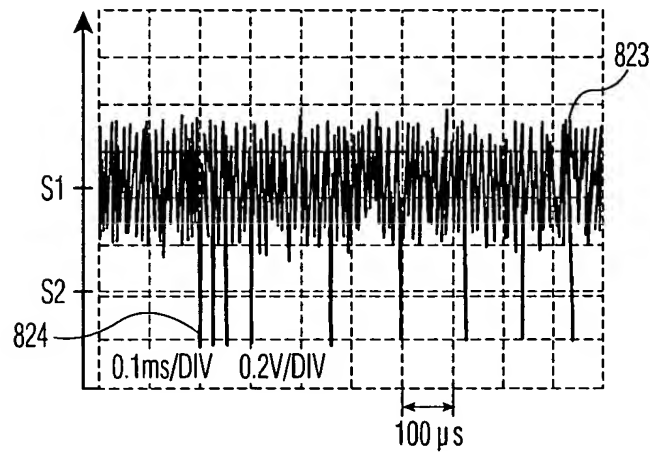


FIG. 9C

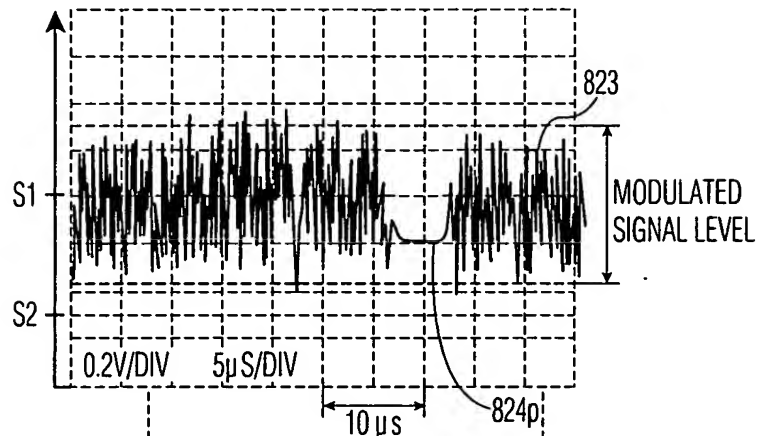
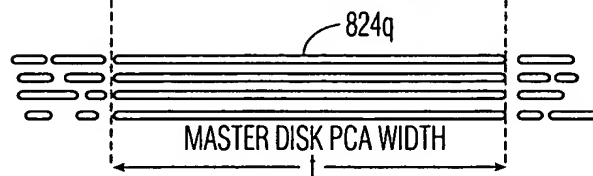


FIG. 9D



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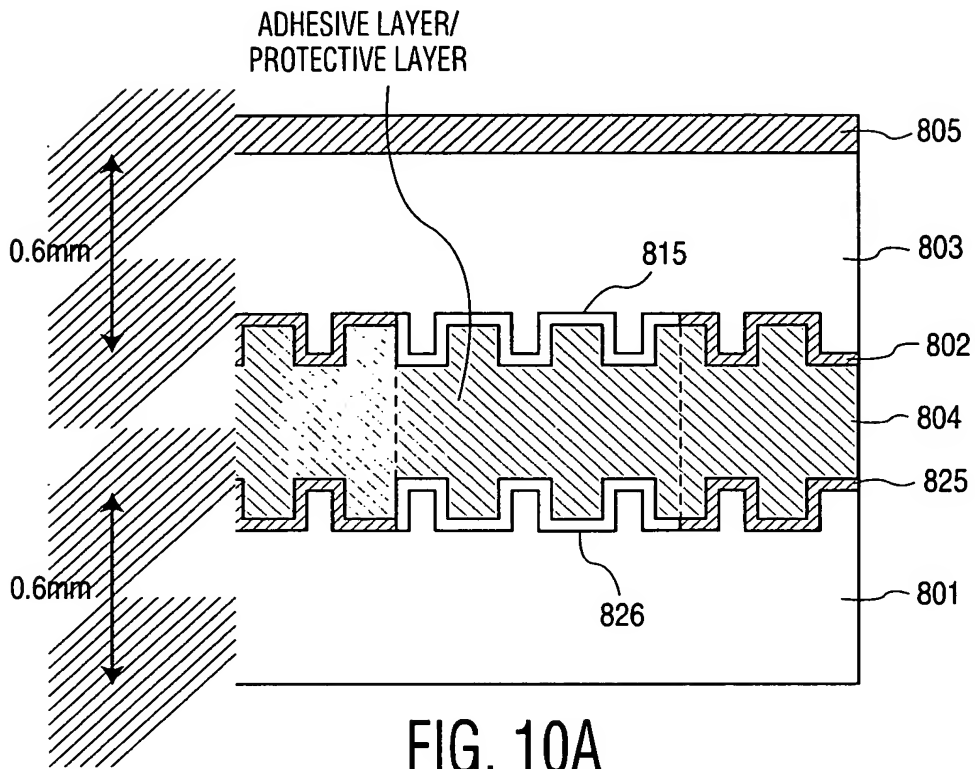


FIG. 10A

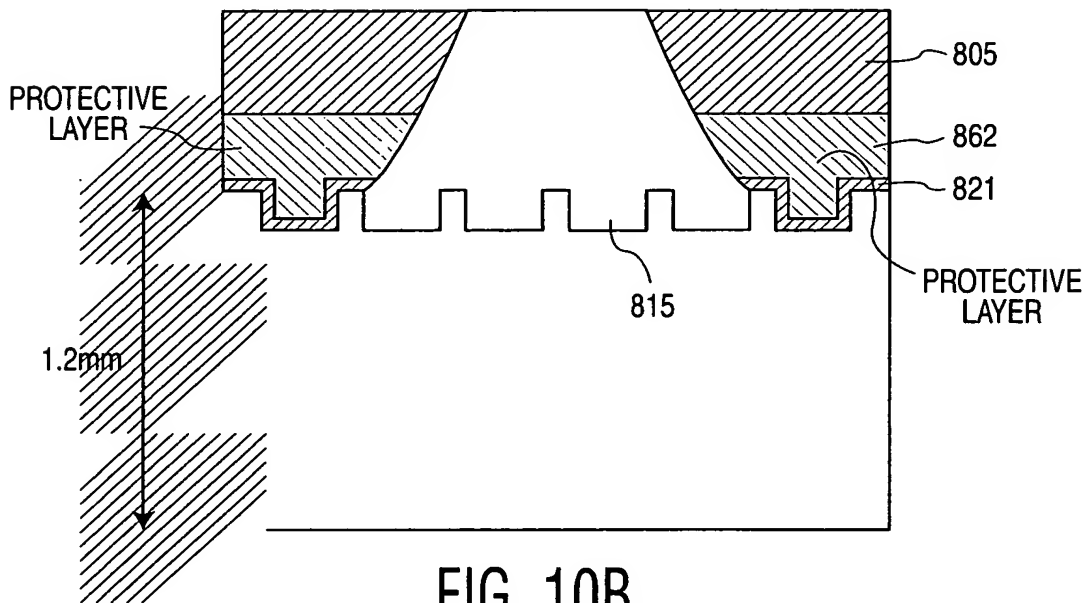


FIG. 10B

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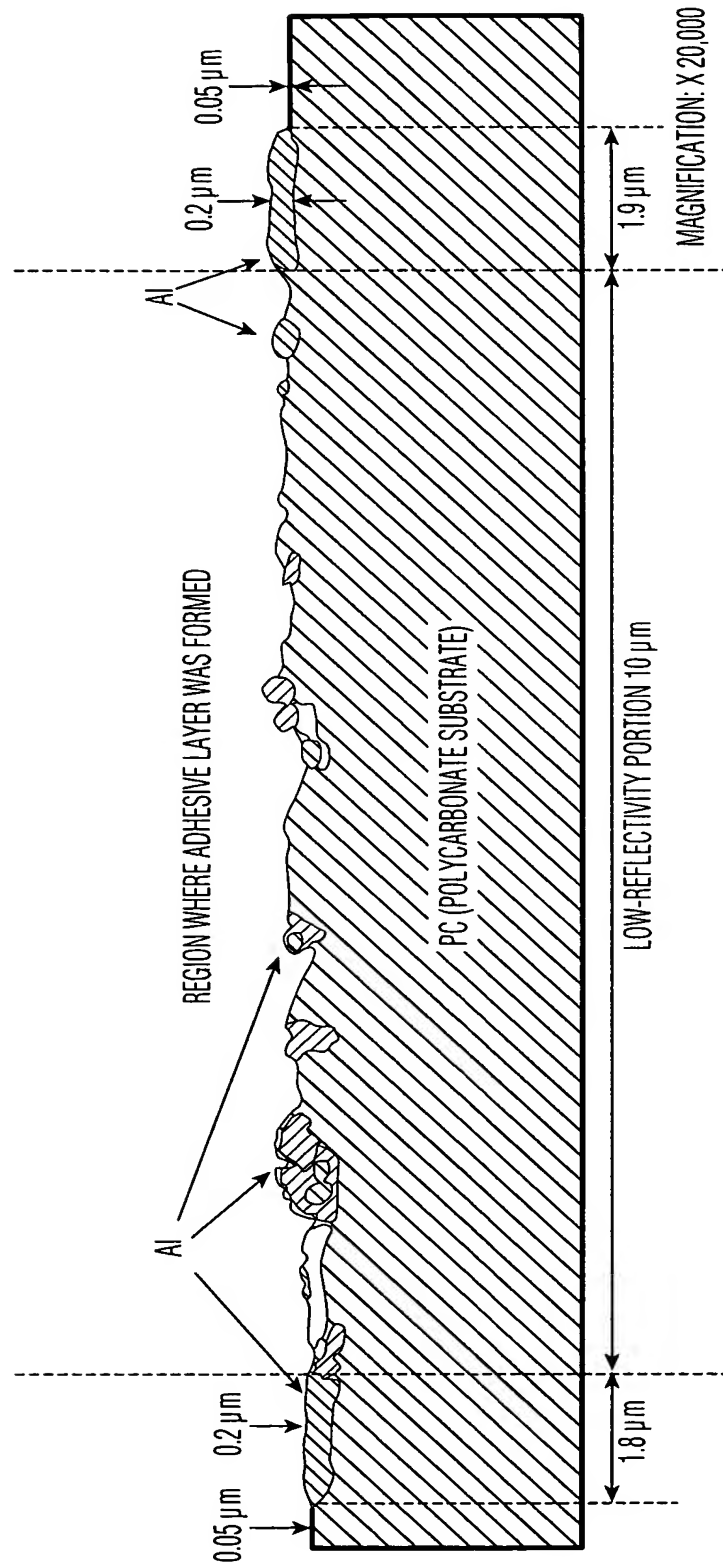


FIG. 11

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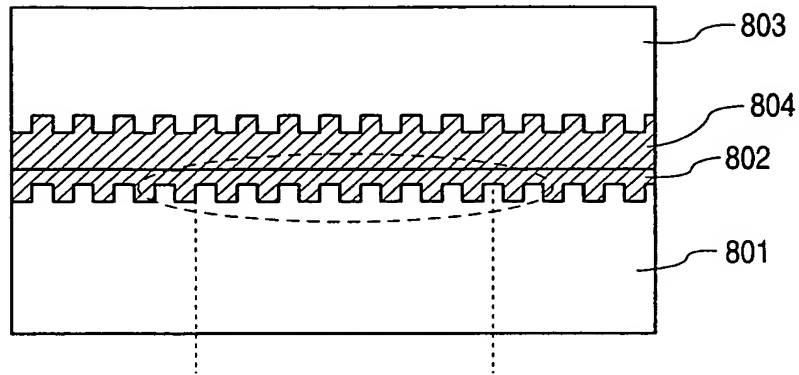


FIG. 12A

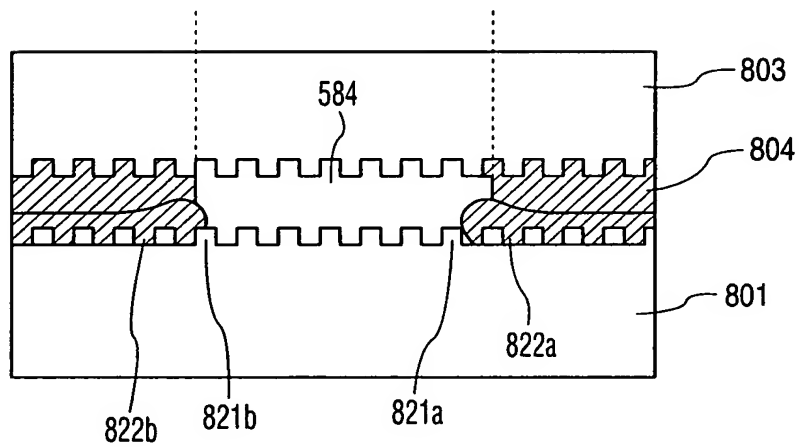


FIG. 12B

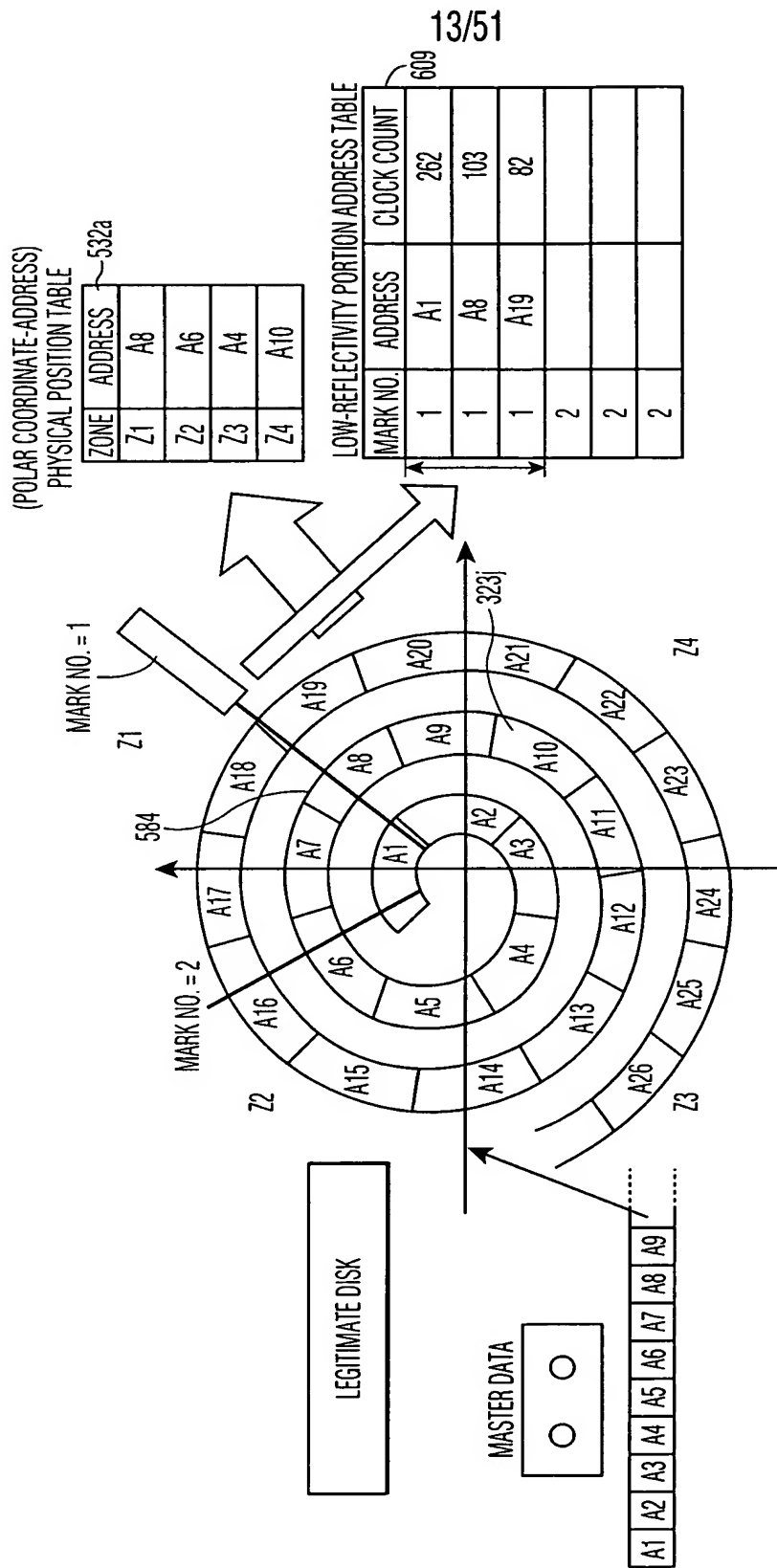


FIG. 13A

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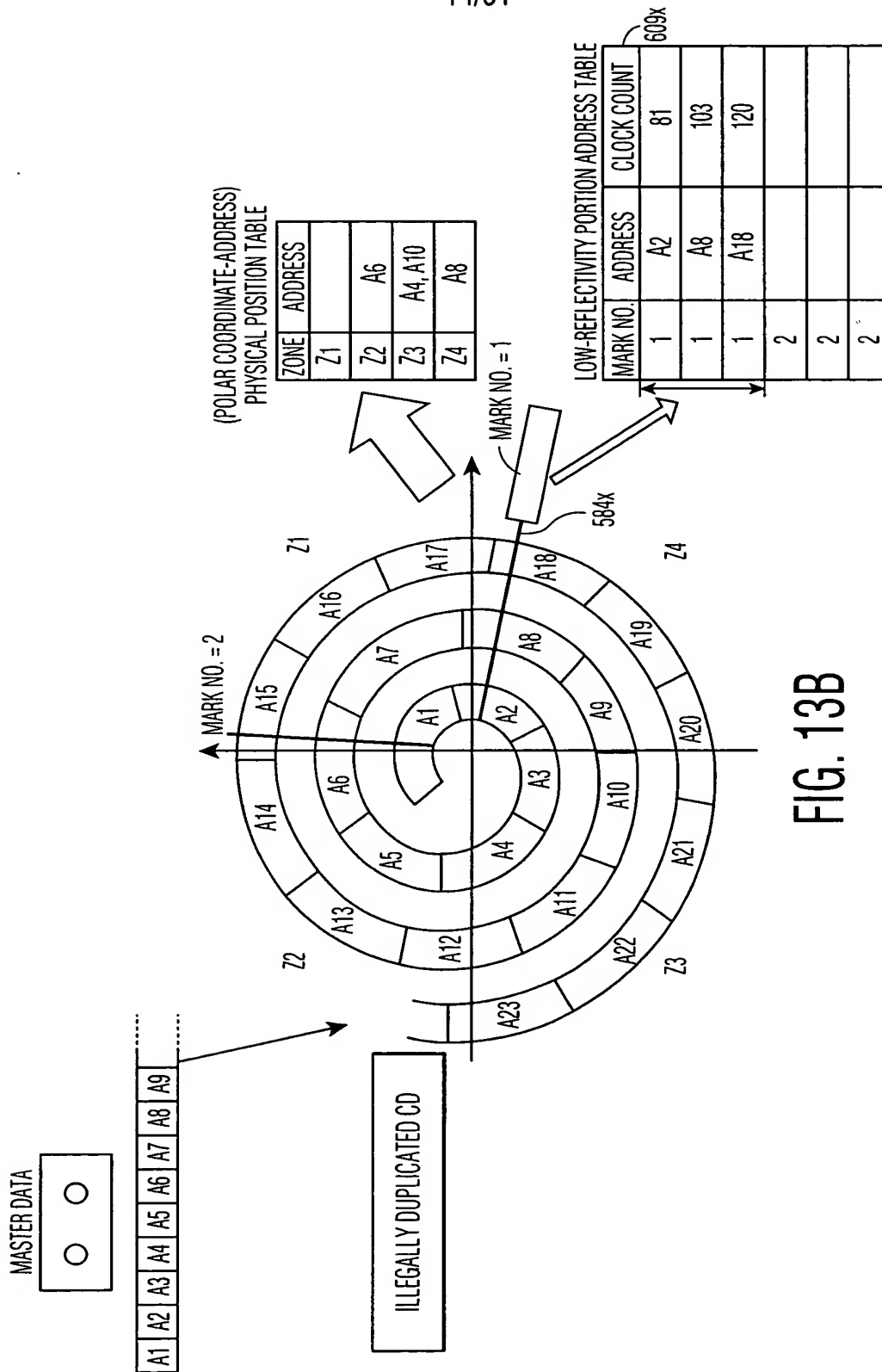


FIG. 13B

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FIG. 14A  
 FIG. 14B

FIG. 14C  
 FIG. 14D

FIG. 14

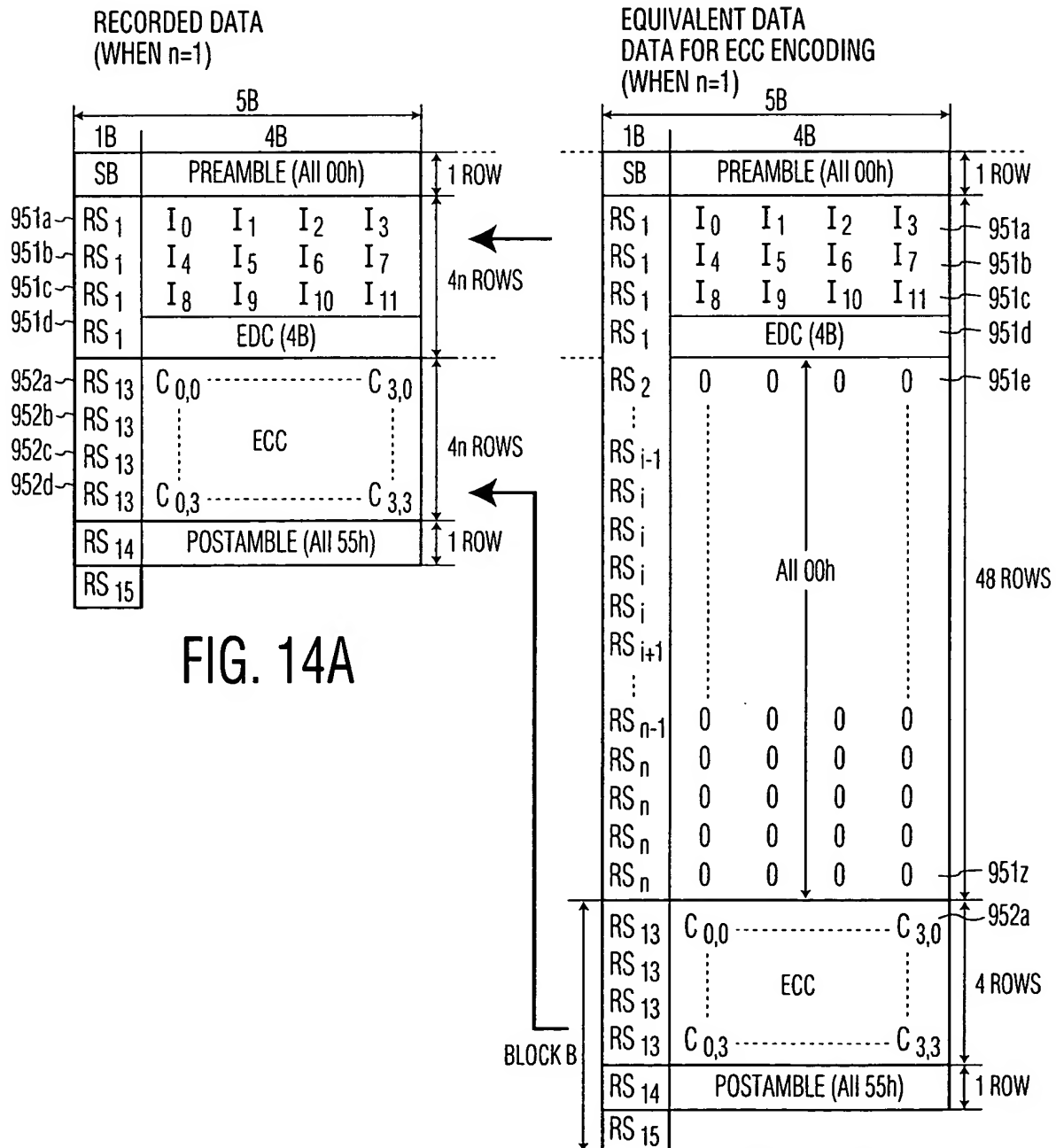


FIG. 14A

FIG. 14B

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TYPICAL EQUATION  
FOR EDC COMPUTATION  
EDC (ERROR DETECTION CODE) :

$$\text{EDC}_{\text{PCA}}(x) = \sum_{i=0}^{31} b_i \cdot x^i$$

$$I_{\text{PCA}}(x) = \sum_{i=32}^{128n-31} b_i \cdot x^i$$

FIG. 14C

TYPICAL EQUATION  
FOR EDC COMPUTATION  
ECC (ERROR CORRECTION CODE) :

$$R_{\text{PCA}}(x) = \sum_{i=48}^{51} I_{j+4i} \cdot x^{51-i}$$

$$I_{\text{PCA}}(x) = \sum_{i=0}^{4n-2} I_{j+4i} \cdot x^{51-i} + D_j \cdot x^{52-4n},$$

FIG. 14D



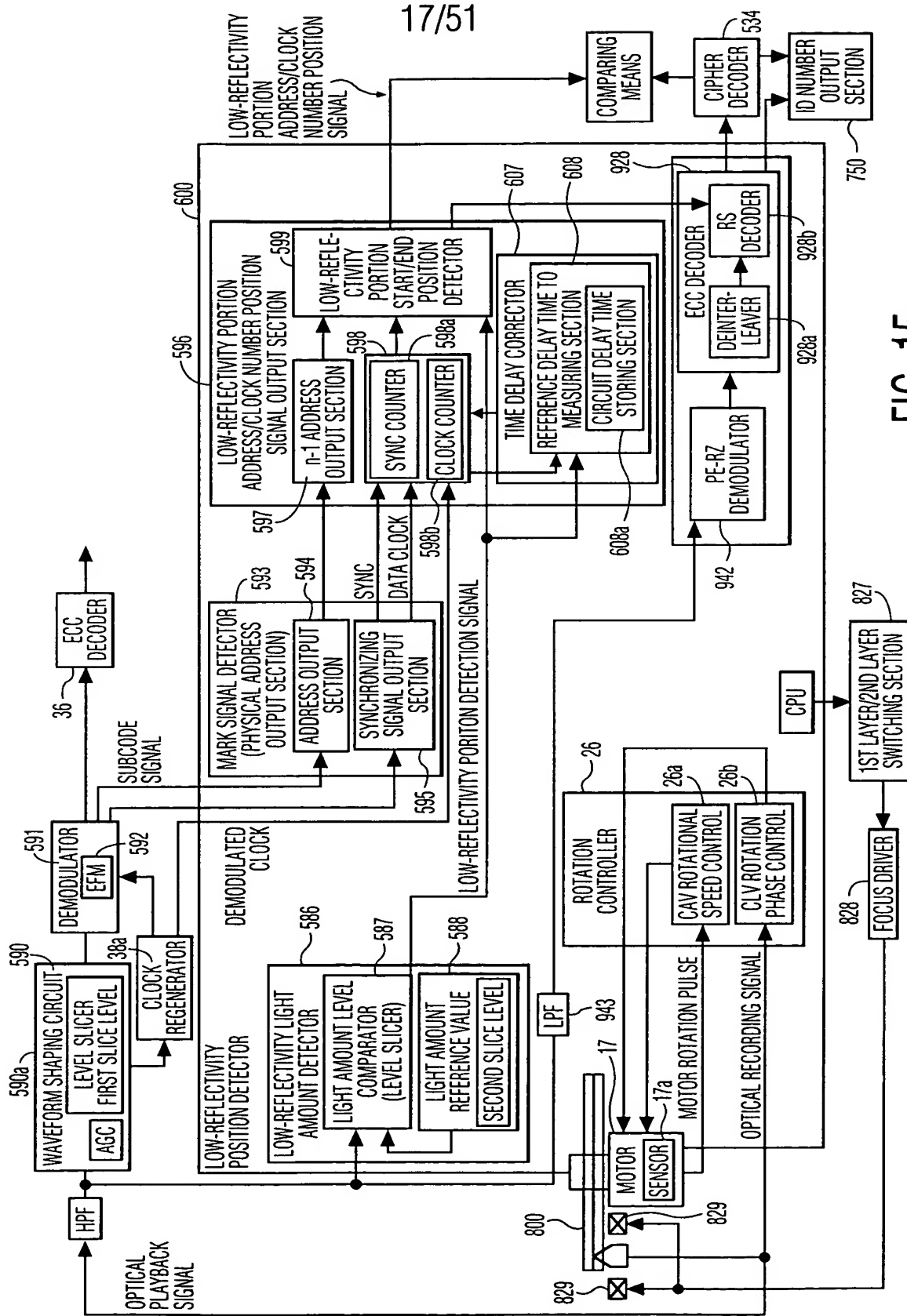


FIG. 15

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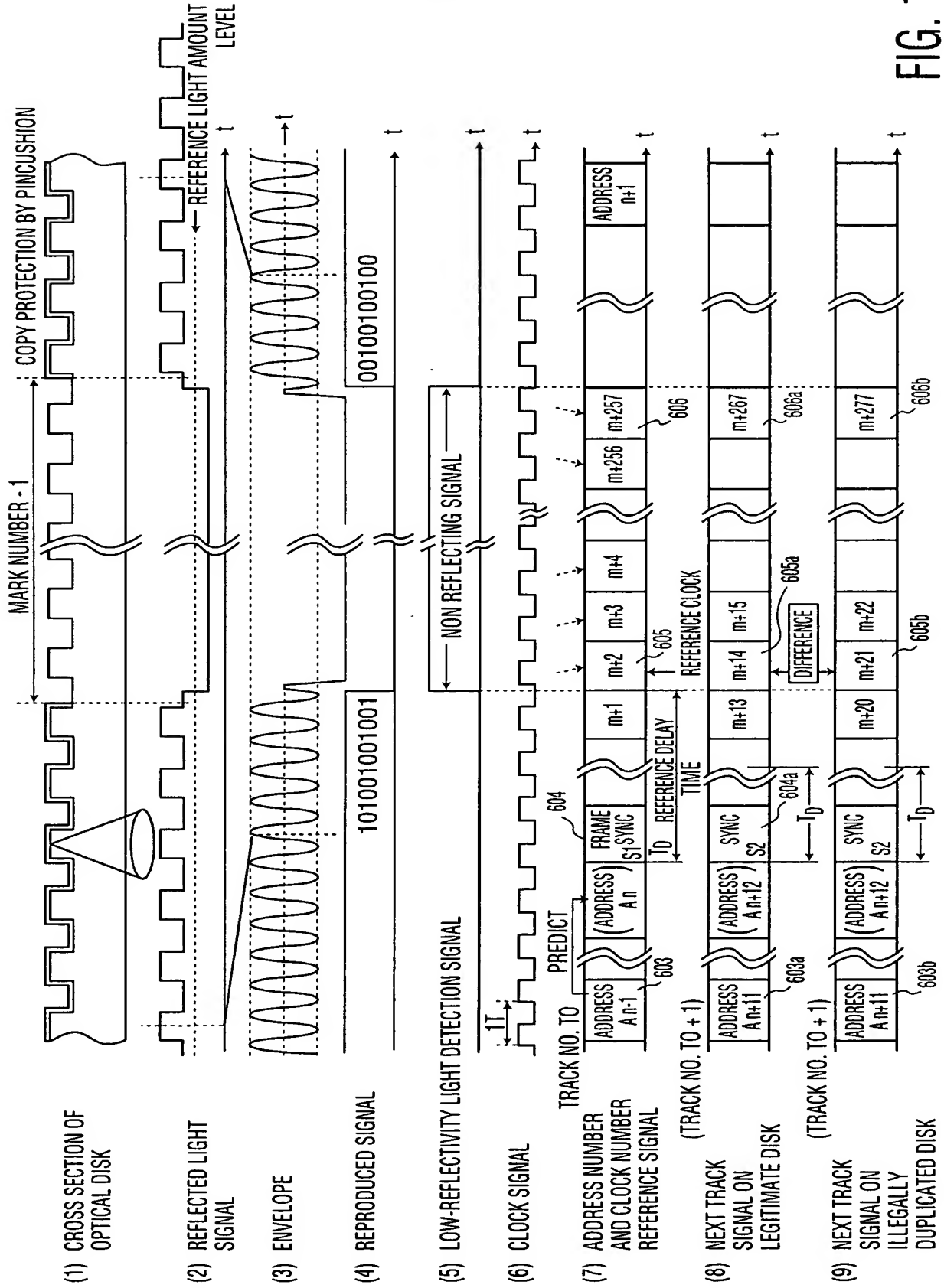


FIG. 16

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LEGITIMATE DISK

LOW-REFLECTIVITY PORTION ADDRESS TABLE

MARK NO.	START POSITION			END POSITION		
	ADDRESS	SYNC NO	CLOCK NUMBER	ADDRESS	SYNC NO	CLOCK NUMBER
1	A n	S1	m+2	n		m+257
1	A n+12	S2	m+14	n+12		m+267
1	A n+23		m+25	n+23		m+300
:	:		:	:		:
2	A n+1		m+15	n+1		m+160
2	A n+13		m+85	n+13		m+250
2	A n+24		m+68	n+24		m+210
0	A n+9					
0						

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PLANNING

ILLEGALLY DUPLICATED DISK

LOW-REFLECTIVITY PORTION ADDRESS TABLE

MARK NO.	START POSITION			END POSITION		
	ADDRESS	SYNC NO	CLOCK NUMBER	ADDRESS	SYNC NO	CLOCK NUMBER
1	n	S1	m+2	n		m+257
1	n+12	S2	m+21	n+12		m+277
1	n+22		m+4	n+22		m+230
:	:		:	:		:
2	n+1		m+36	n+1		m+190
2	n+13		m+120	n+13		m+281
2	n+25			n+25		
0	n+9					
0						

PLANNING

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FIG. 17

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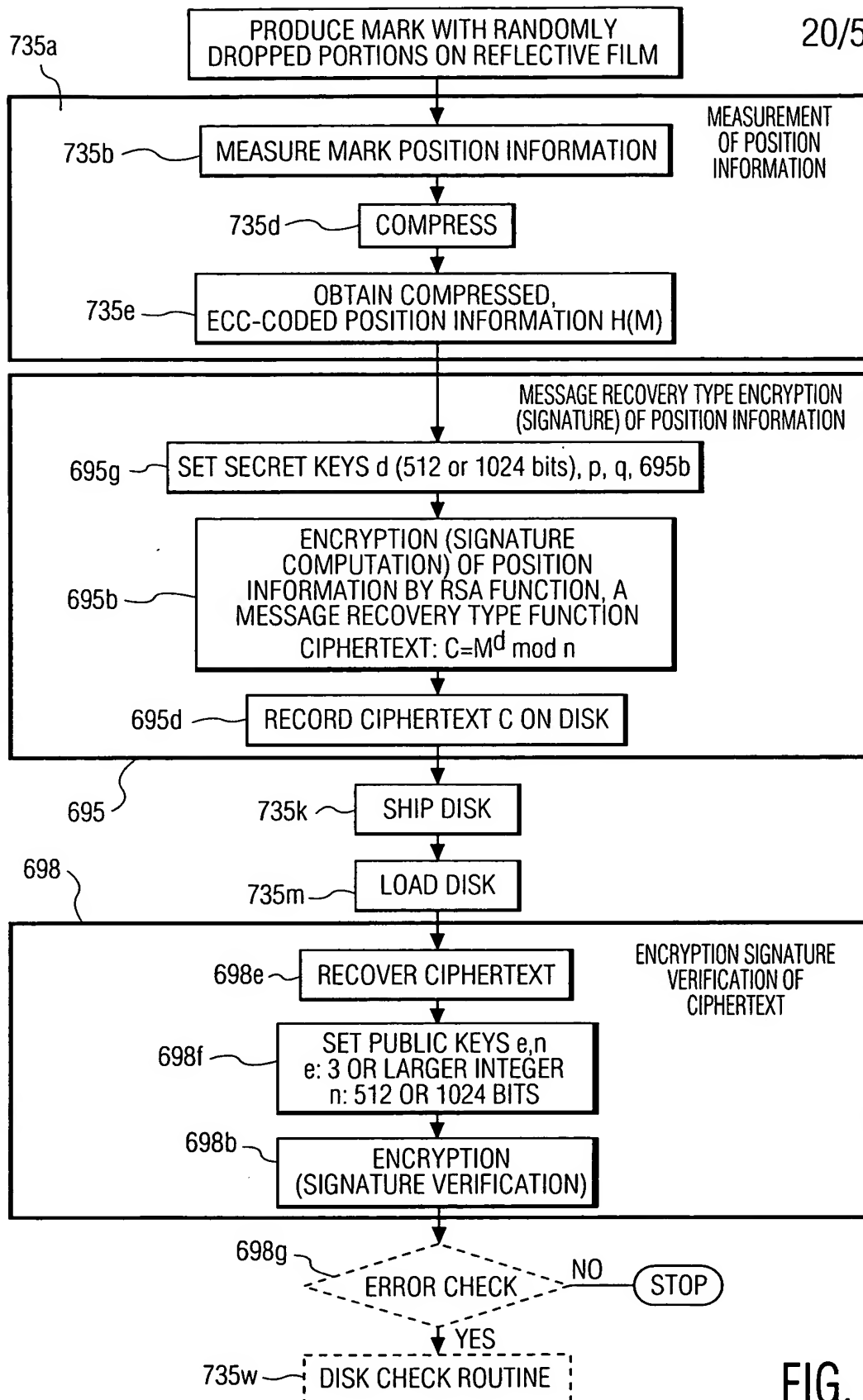


FIG. 18A

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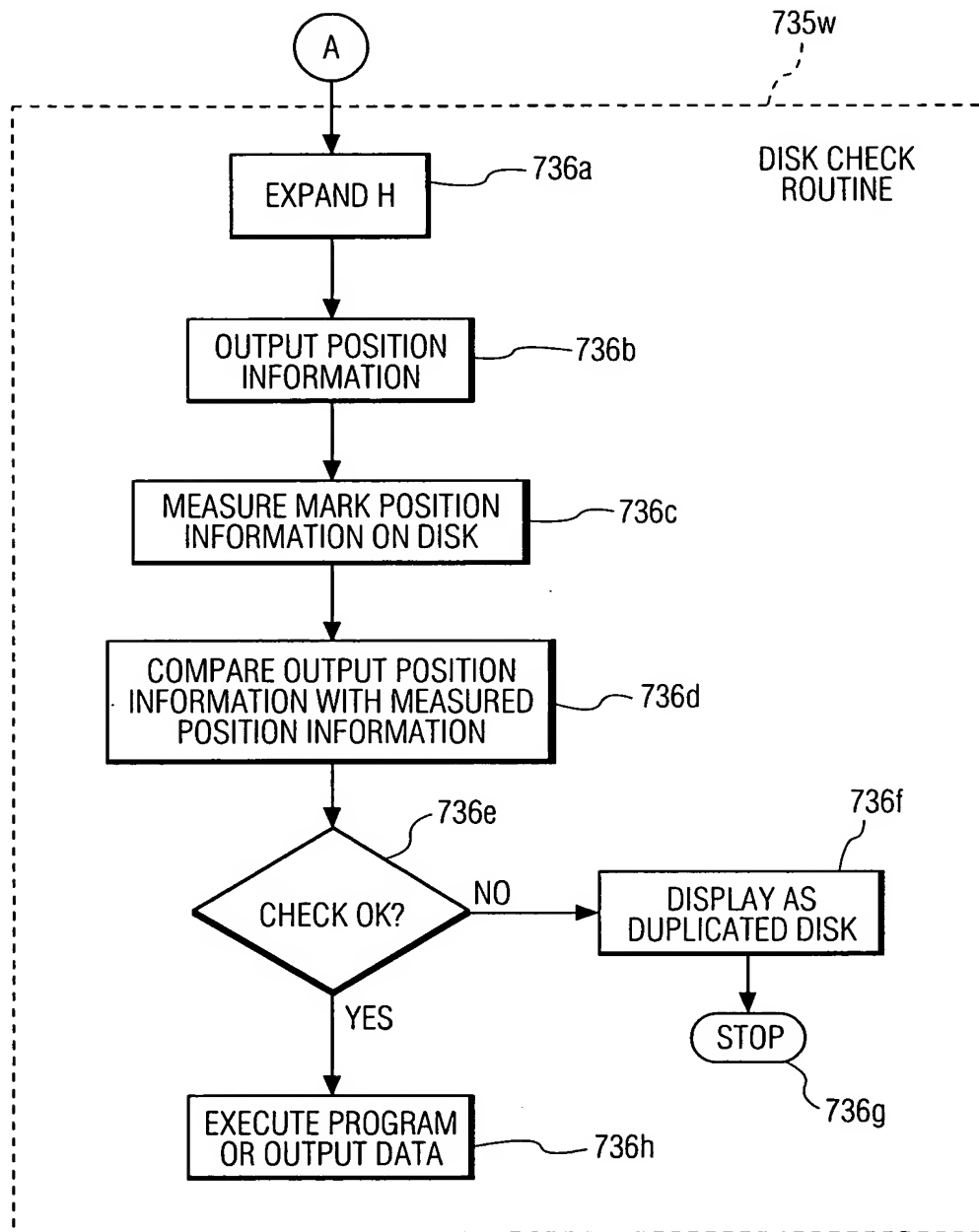


FIG. 18B

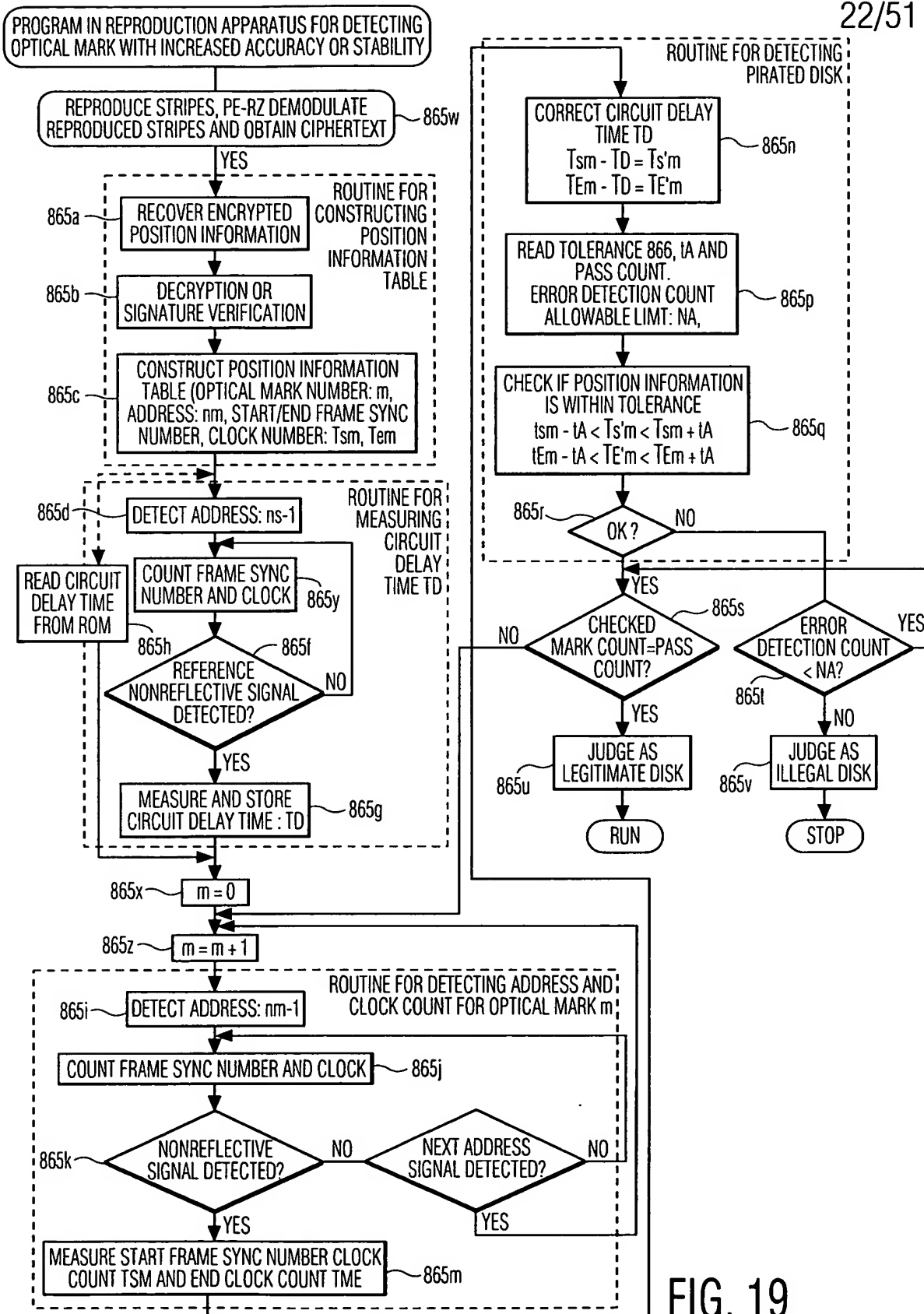
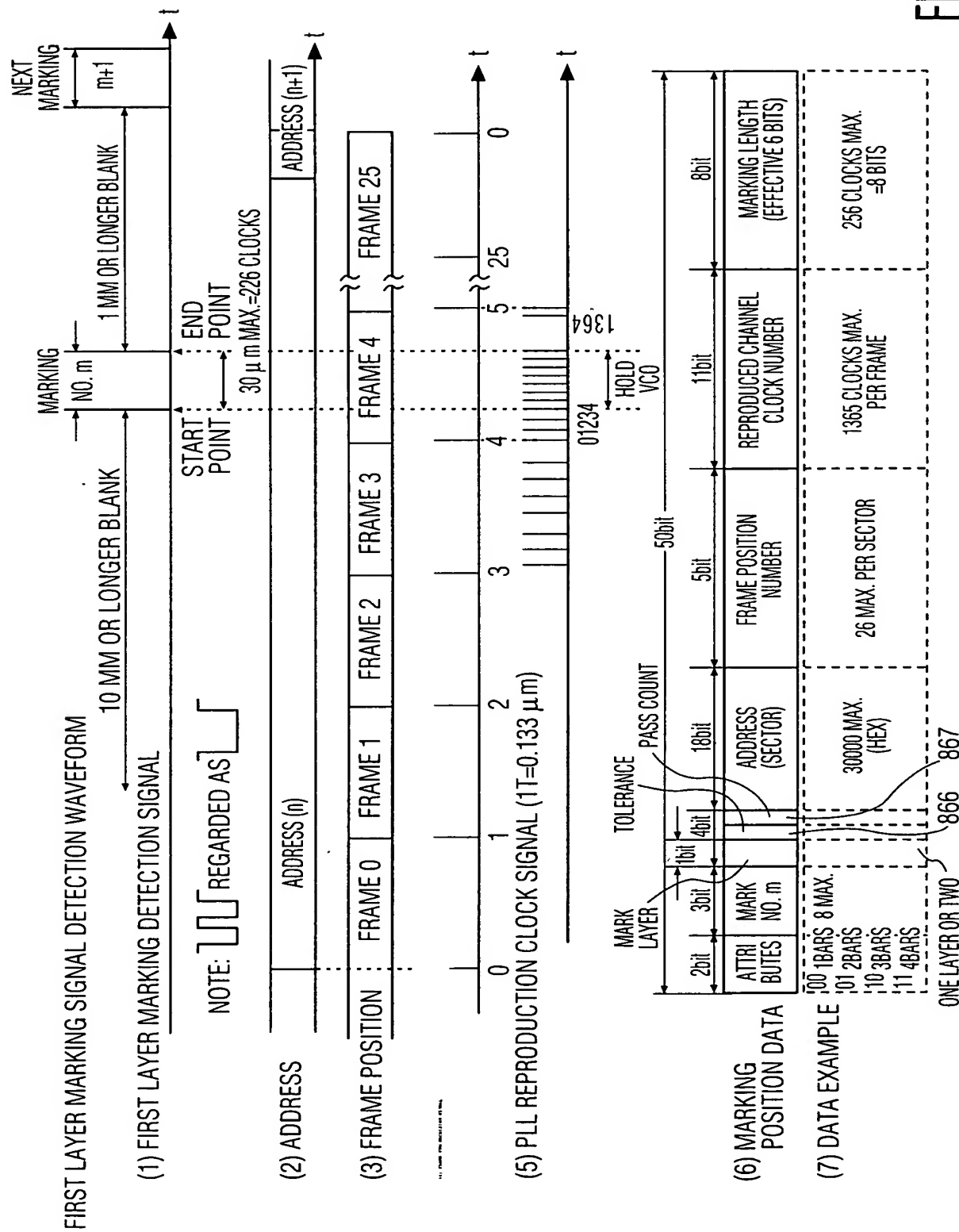
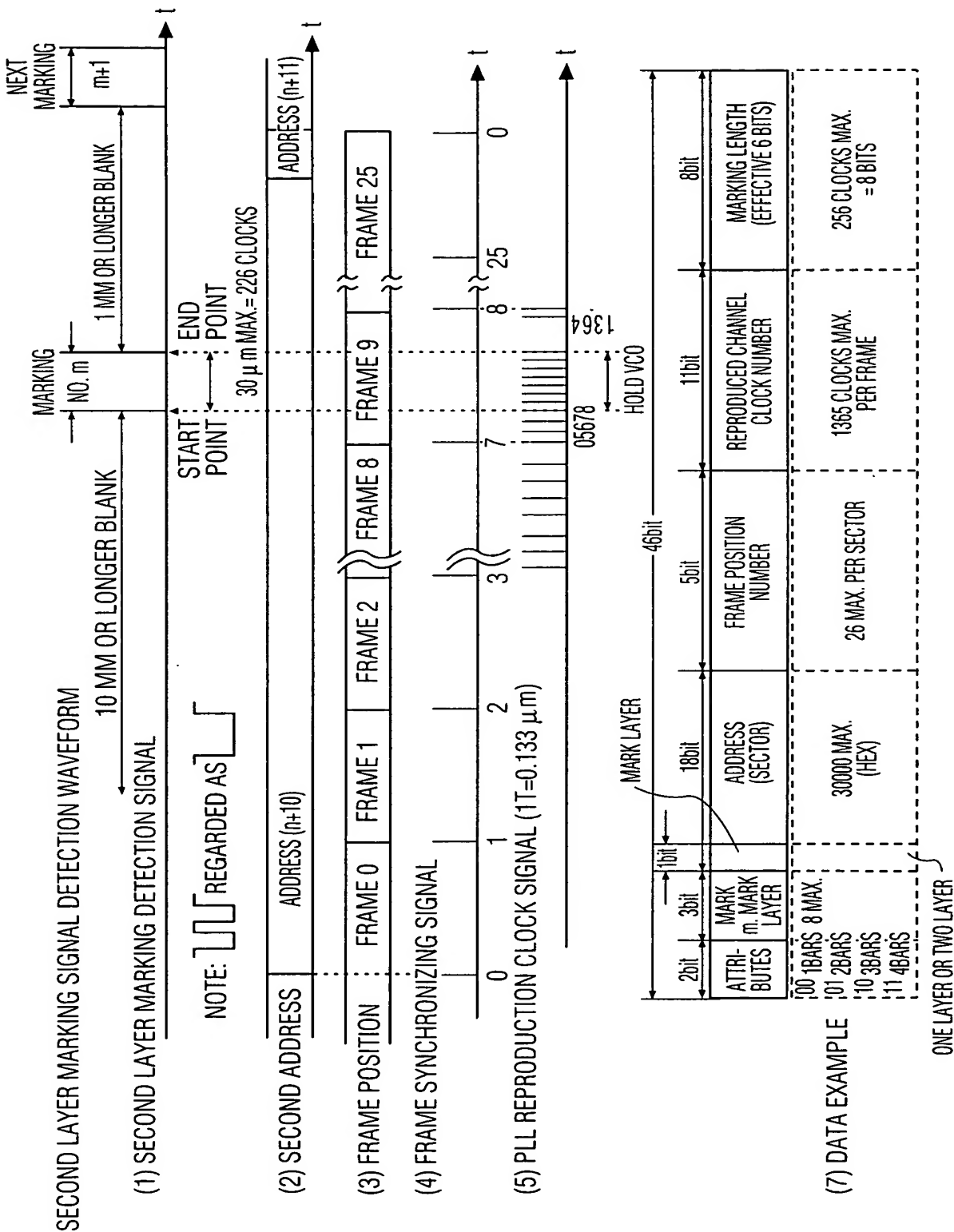


FIG. 19







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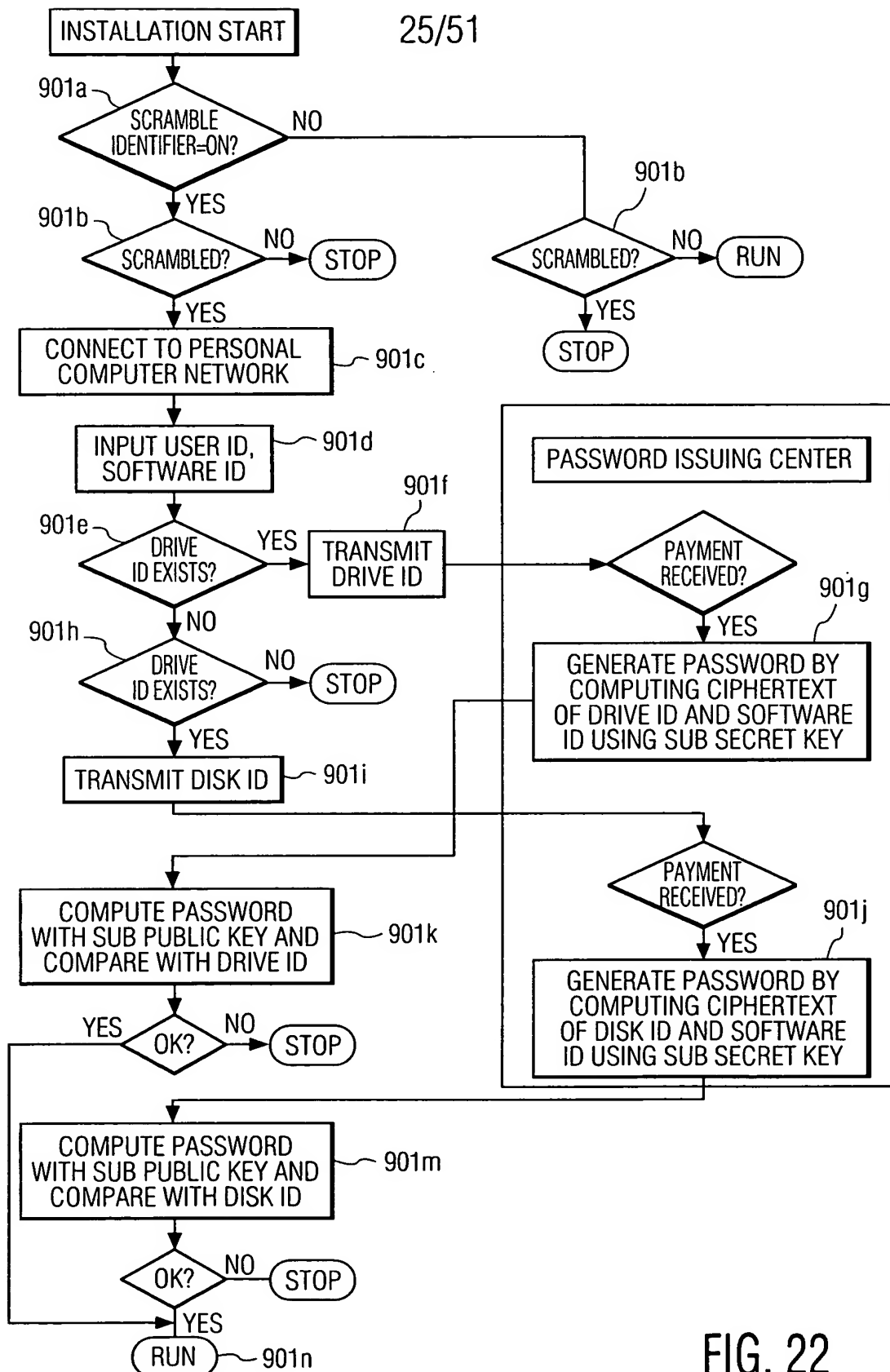


FIG. 22

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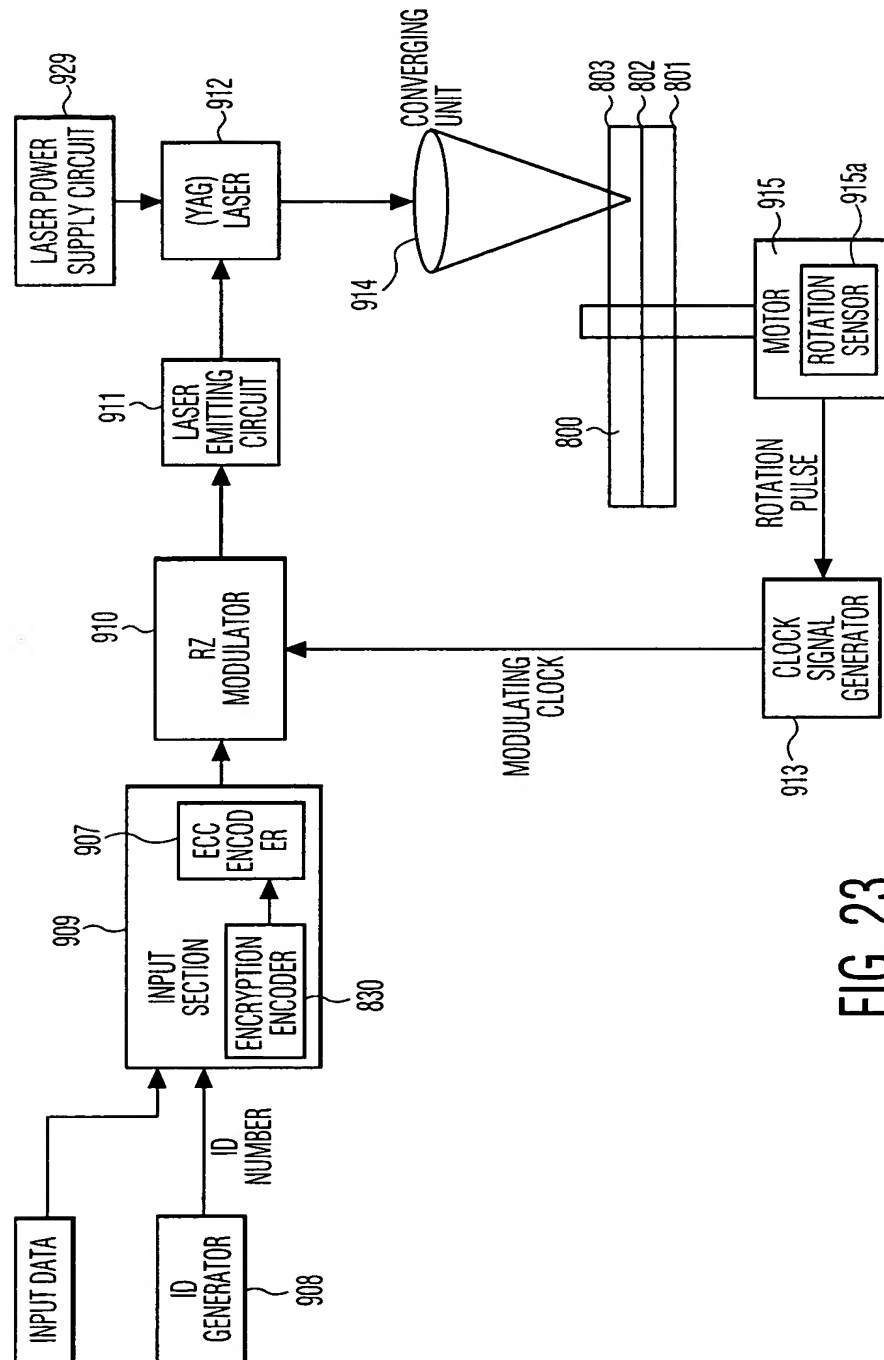
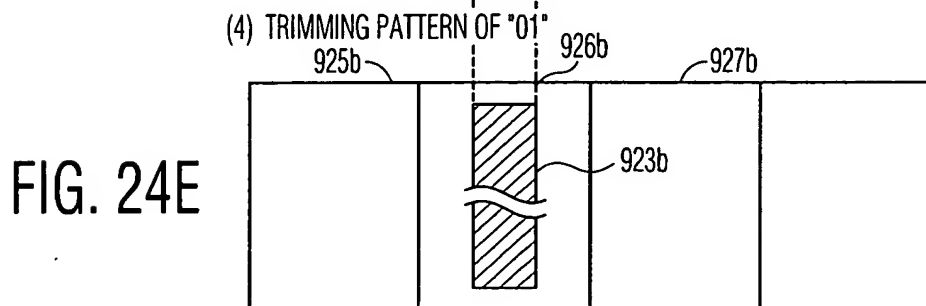
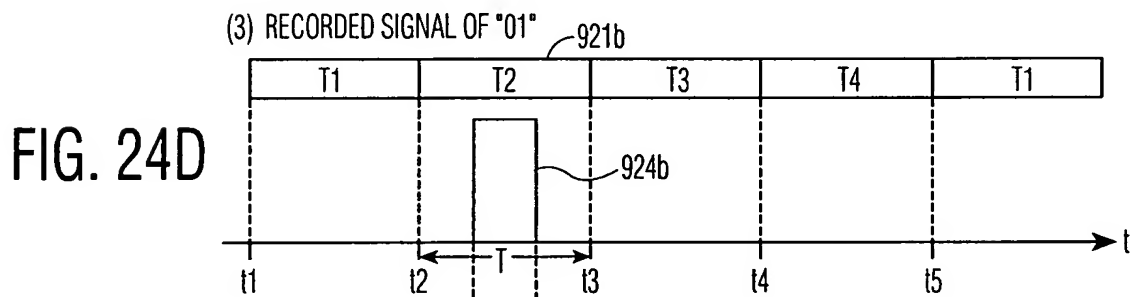
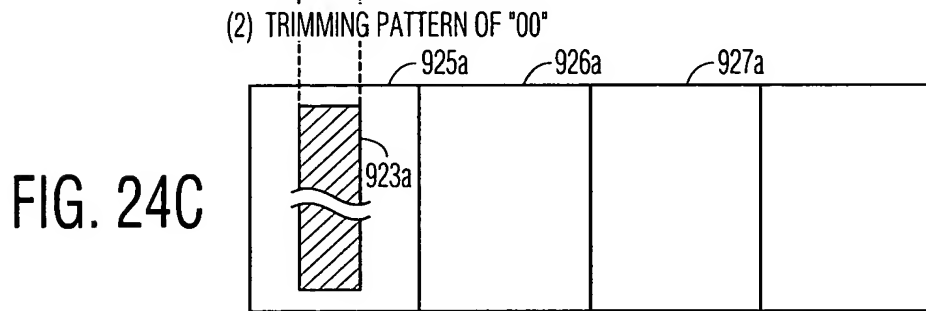
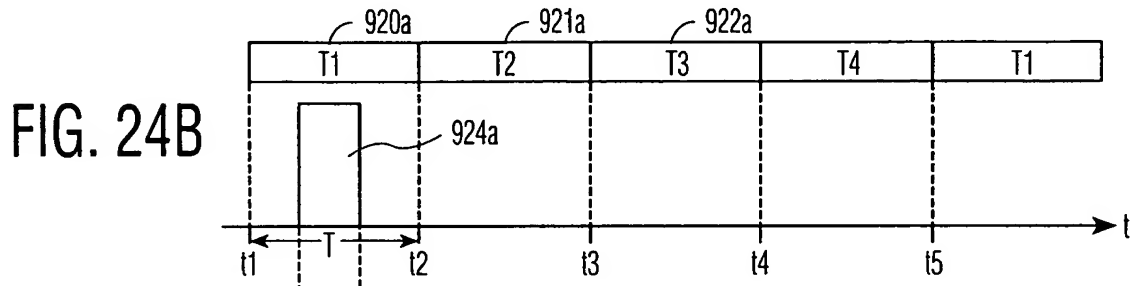


FIG. 23

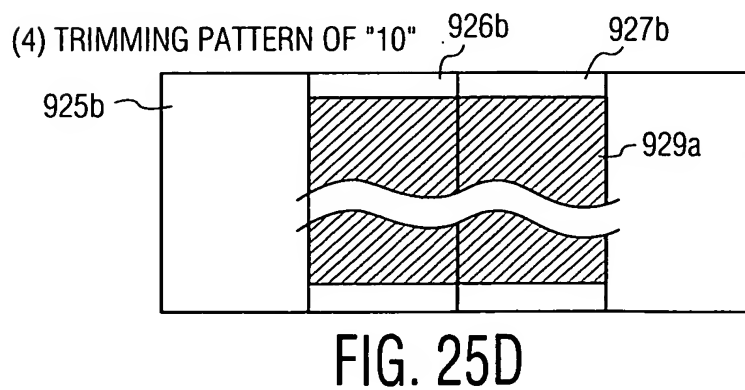
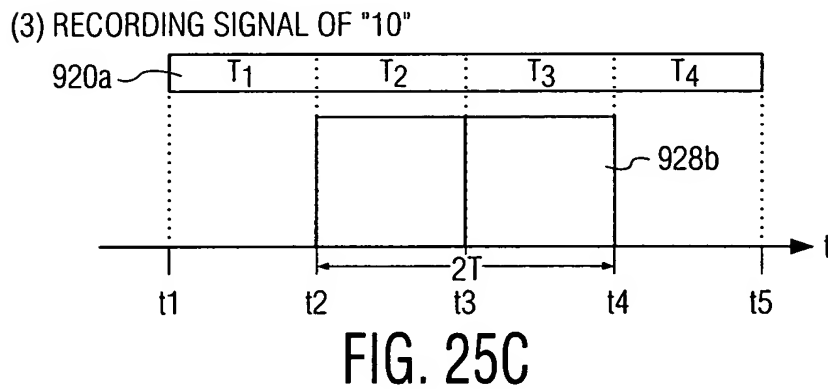
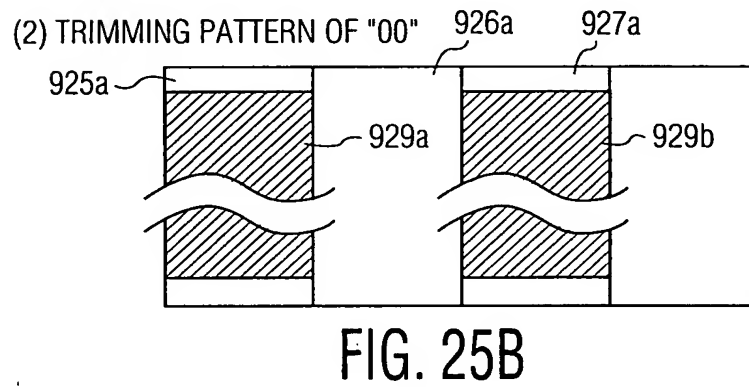
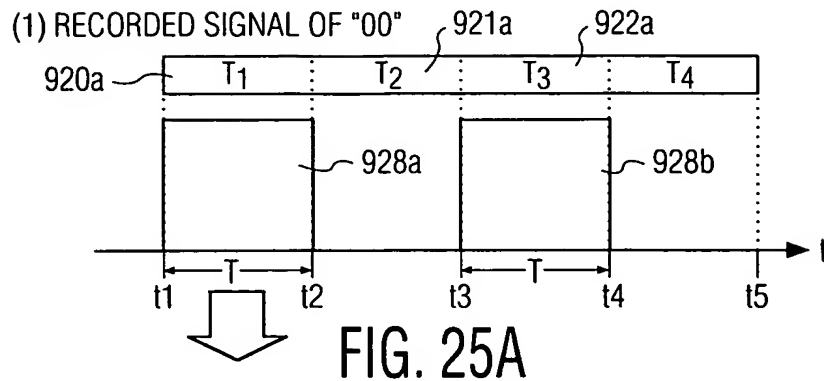
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RZ RECORDING  
 MODULATION CLOCK  
 BASED ON ROTATION  
 PULSE

FIG. 24A (1) RECORDED SIGNAL OF "00"



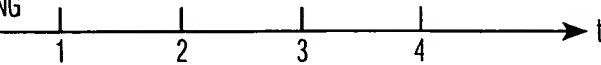
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PE-RZ RECORDING

RECORDING  
 CLOCK



(1) RECORDED SIGNAL OF "0"

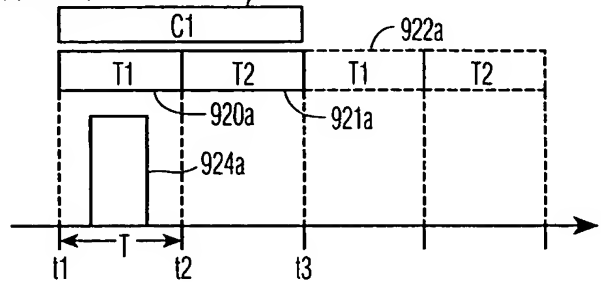


FIG. 26A

(2) TRIMMING PATTERN OF "0"

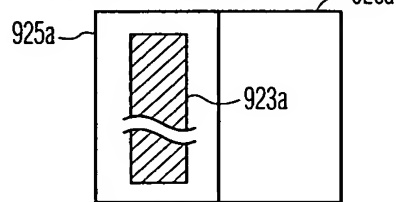


FIG. 26B

(3) RECORDED SIGNAL OF "1"

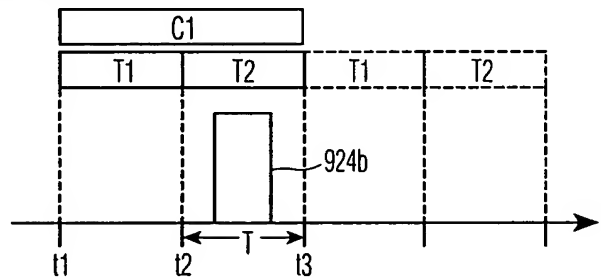


FIG. 26C

(4) TRIMMING PATTERN OF "1"

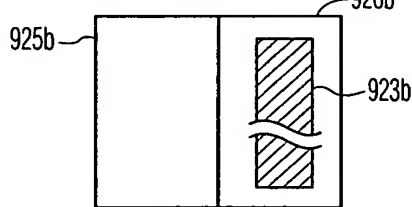


FIG. 26D

(4) RECORDED SIGNAL OF "010"

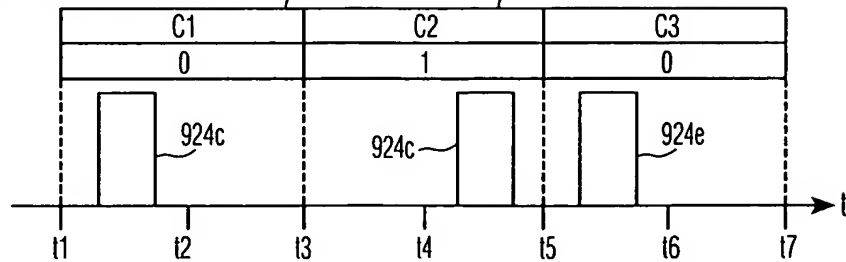


FIG. 26E

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(1) TOP PLAN VIEW

FIG. 27A

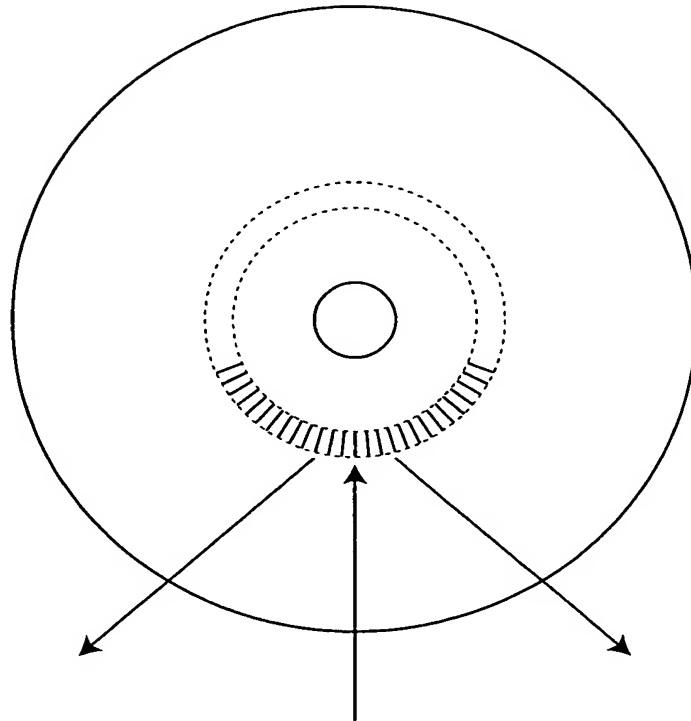


FIG. 27B

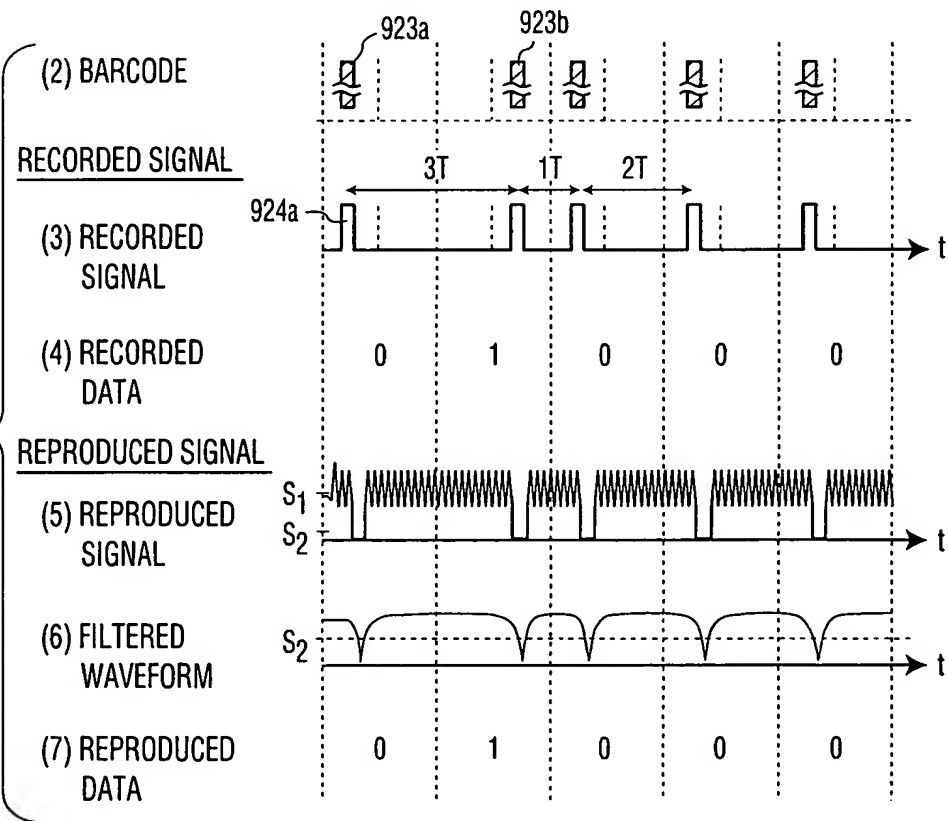


FIG. 28A

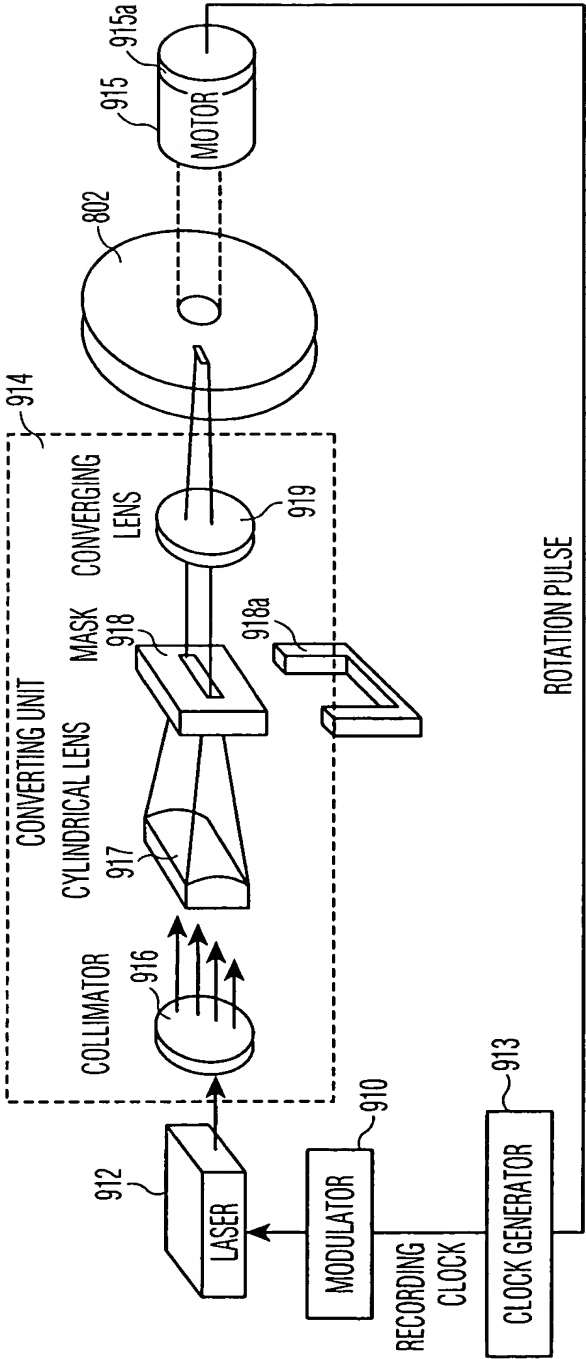
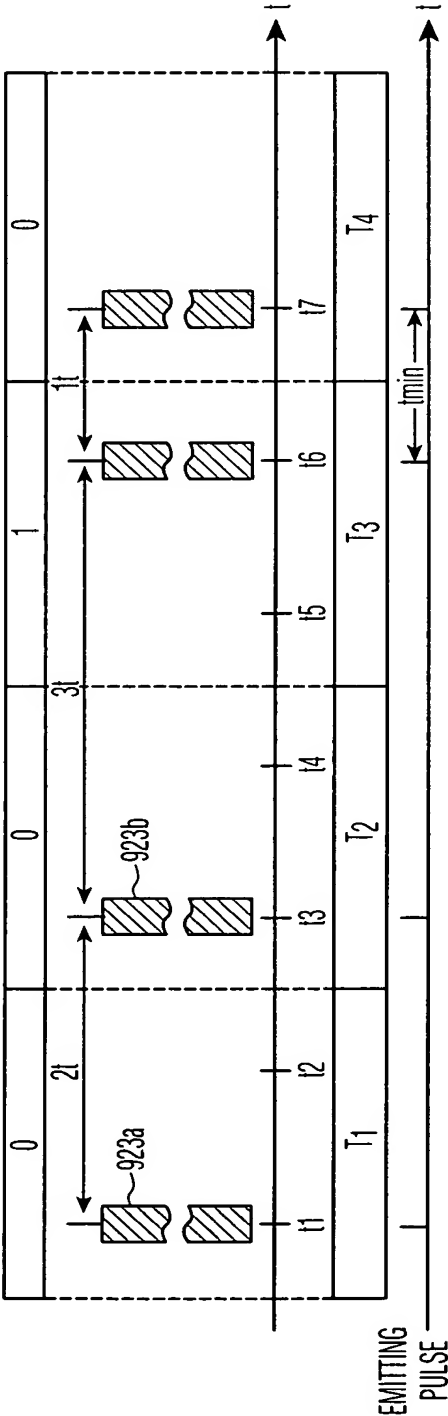
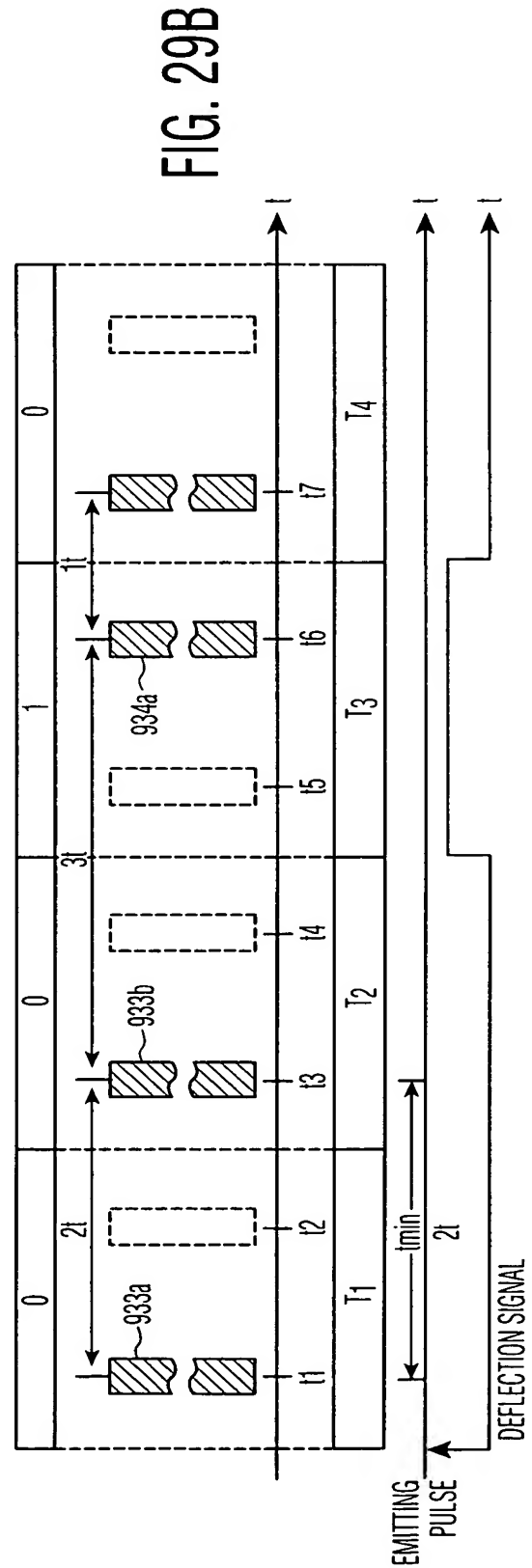
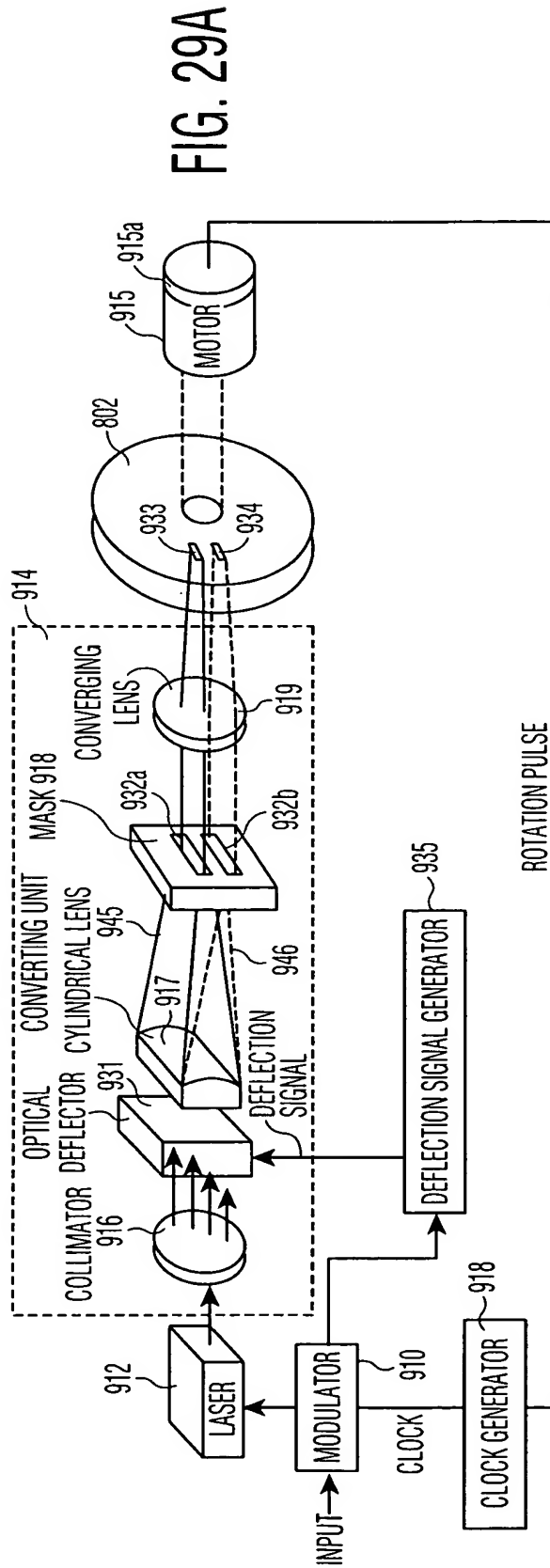


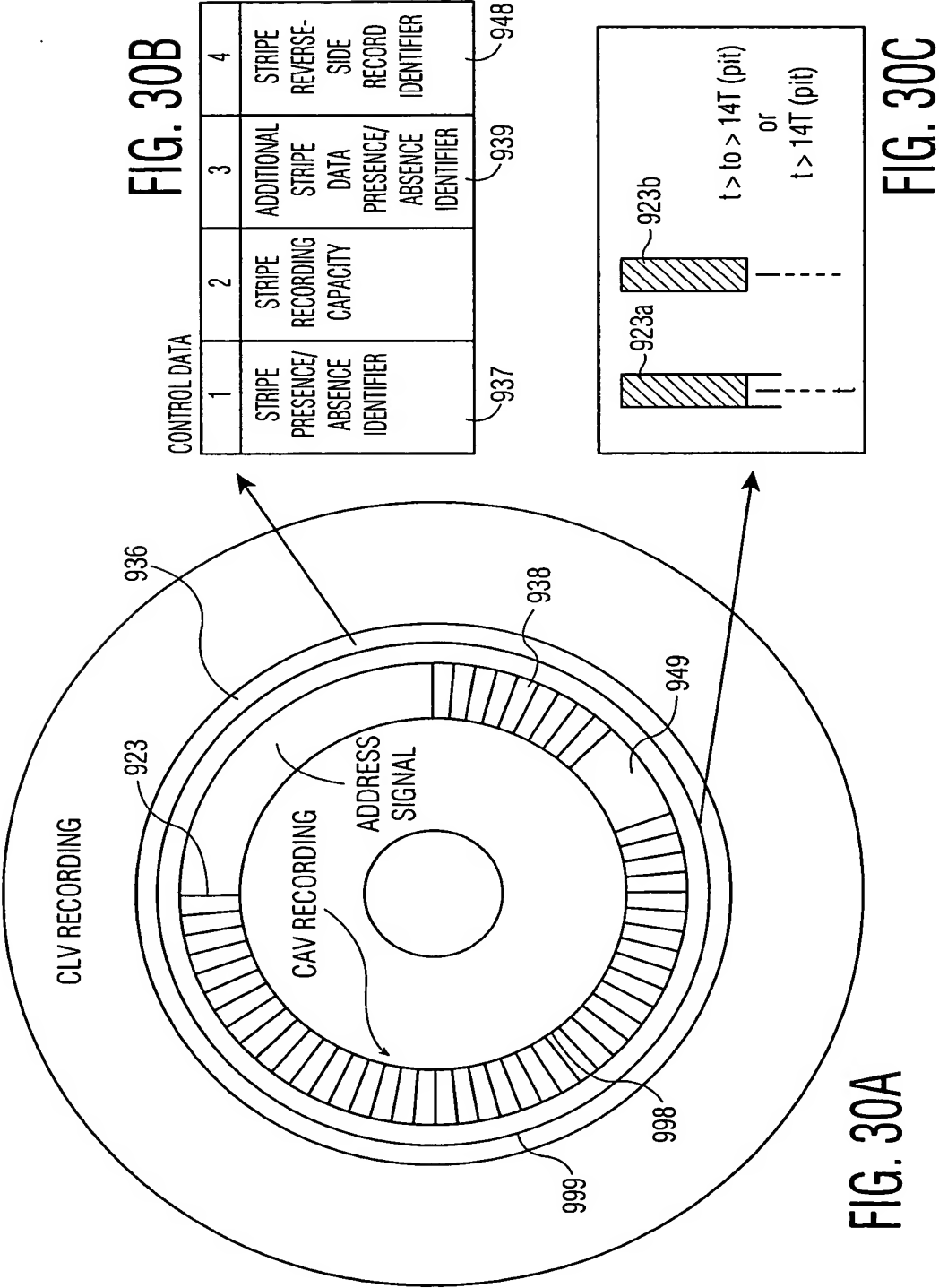
FIG. 28B



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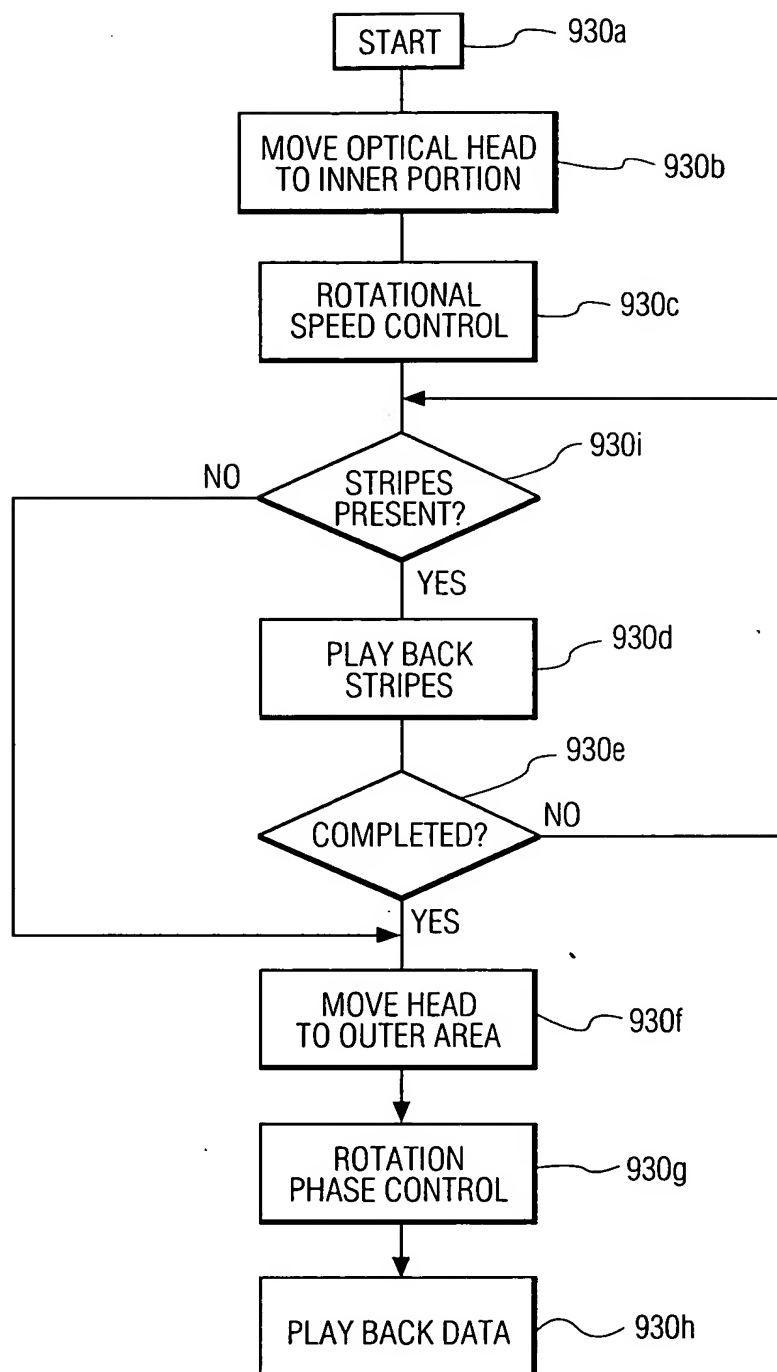


FIG. 31

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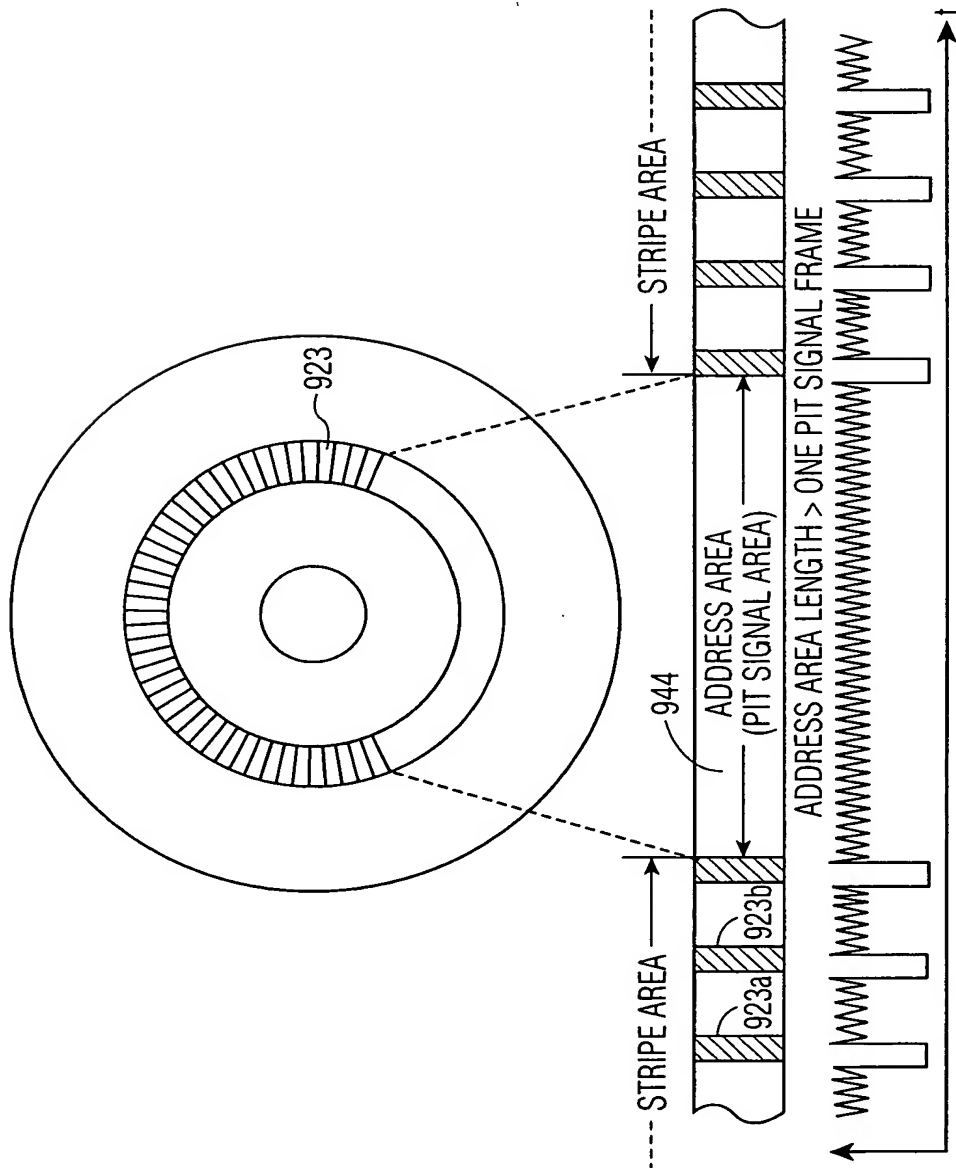


FIG. 32

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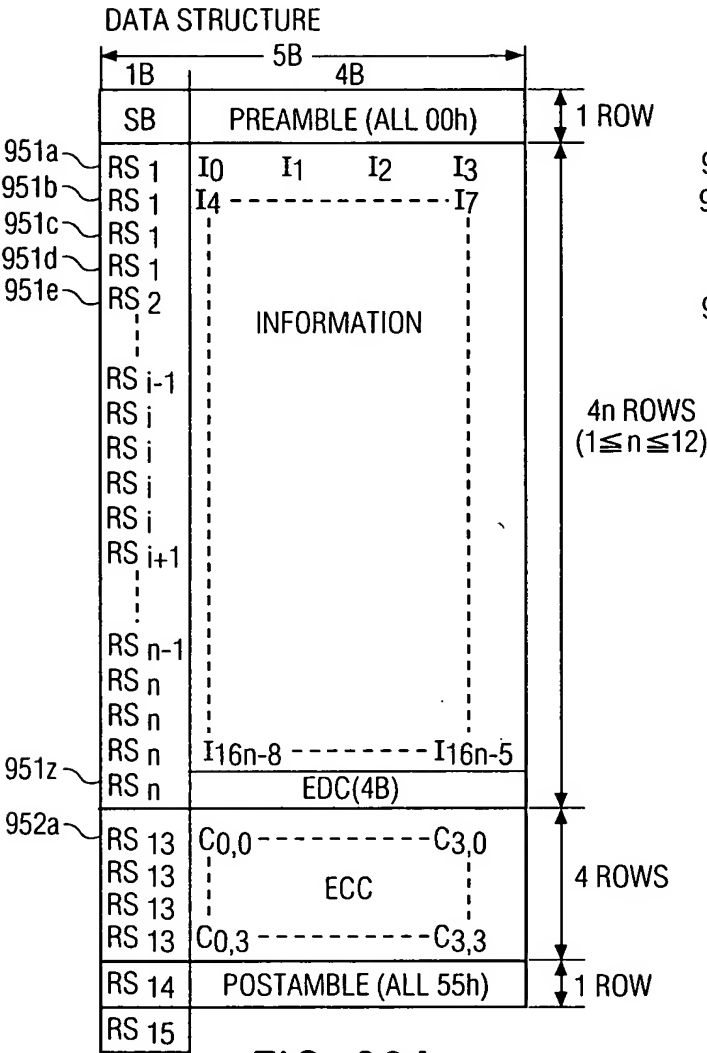


FIG. 33A

DATA STRUCTURE WHEN n=1

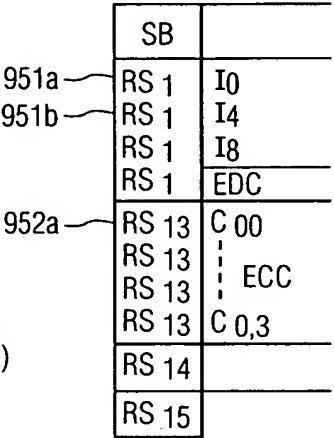


FIG. 33B

RANDOM ERROR CORRECTION CAPABILITY	
BIT ERROR RATE BEFORE CORRECTION	READ ERROR RATE AFTER CORRECTION
10 <sup>-5</sup>	1 IN 10 <sup>10</sup> DISKS
10 <sup>-4</sup>	1 IN 10 <sup>7</sup> DISKS
10 <sup>-3</sup>	1 IN 10 <sup>4</sup> DISKS
BURST ERROR CORRECTION CAPABILITY	

FIG. 33C

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SYNCHRONIZATION CODE DATA

SYNCHRONIZATION CODE

SYNC BYTE /RESYNC	BIT PATTERN											
	FIXED PATTERN (CHANNEL BIT)								SYNC CODE (DATA BIT)			
	C <sub>15</sub>	C <sub>14</sub>	C <sub>13</sub>	C <sub>12</sub>	C <sub>11</sub>	C <sub>10</sub>	C <sub>9</sub>	C <sub>8</sub>	b <sub>3</sub>	b <sub>2</sub>	b <sub>1</sub>	b <sub>0</sub>
SB	0	1	0	0	0	1	1	0	0	0	0	0
RS <sub>1</sub>	0	1	0	0	0	1	1	0	0	0	0	1
RS <sub>2</sub>	0	1	0	0	0	1	1	0	0	0	1	0
⋮					⋮					⋮		
RS <sub>i</sub>	0	1	0	0	0	1	1	0			i	
⋮					⋮					⋮		
⋮					⋮					⋮		
RS <sub>15</sub>	0	1	0	0	0	1	1	0	1	1	1	1

FIG. 34A

FIXED SYNCHRONIZATION PATTERN

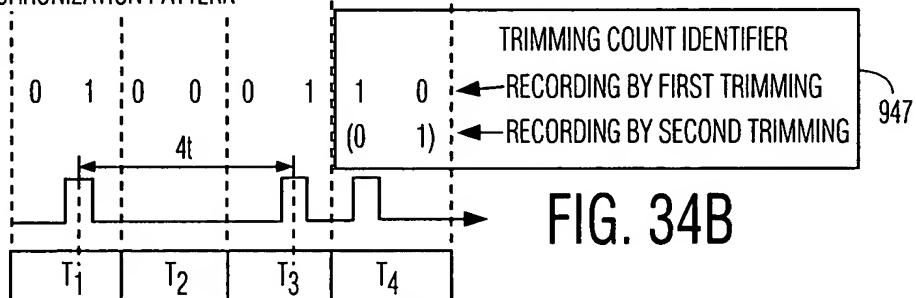


FIG. 34B

MAXIMUM CAPACITY

	RECORDING CAPACITY	TOTAL BYTE COUNT	EFFICIENCY	RECORDING AREA ANGLE	UNRECORDED AREA ANGLE
MINIMUM	12B	41B	29.3%	51 DEGREES	309 DEGREES
MAXIMUM	188B	271B	69.4%	336 DEGREES	24 DEGREES

FIG. 34C

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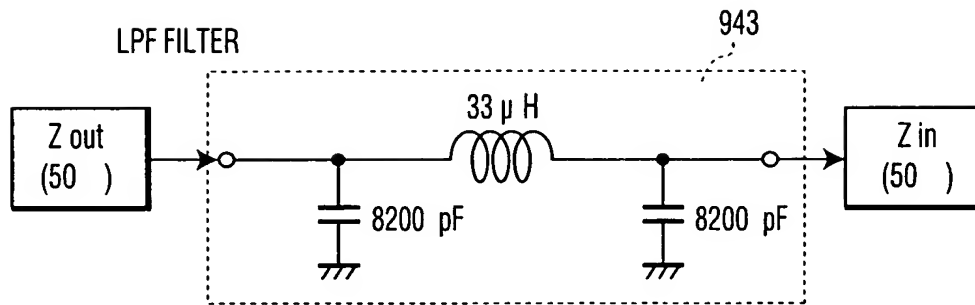


FIG. 35A

SIMULATOR WAVEFORM AFTER LPF :  $I_{14L} = I_S = 0.1$

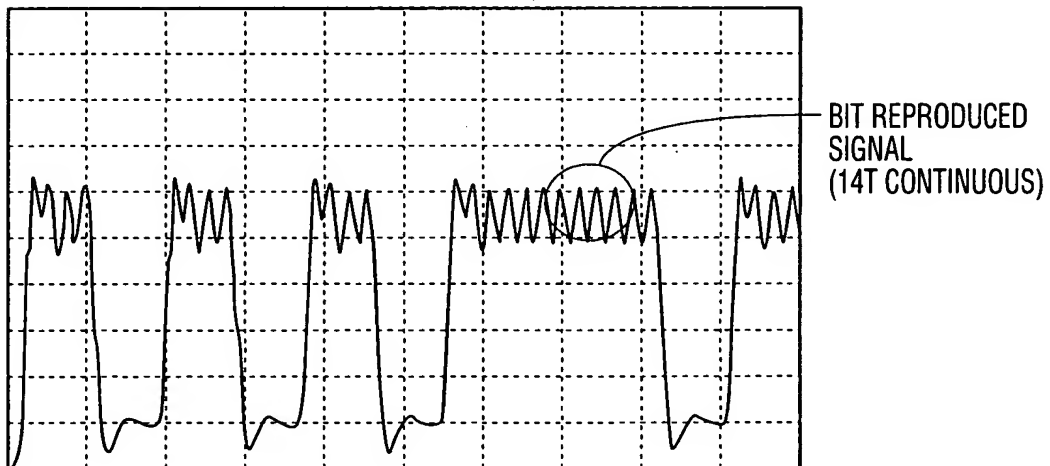


FIG. 35B

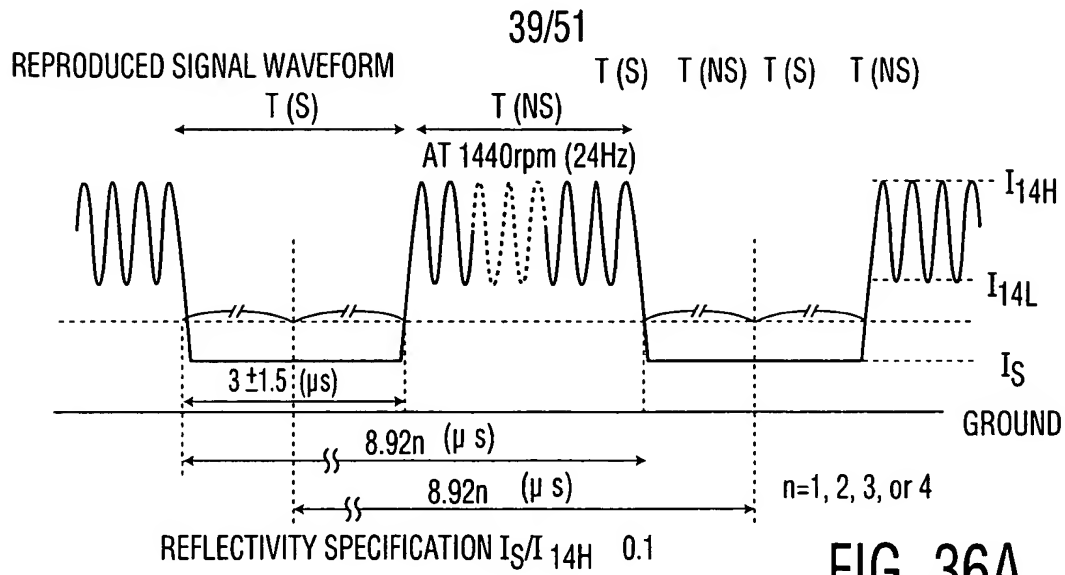


FIG. 36A

DIMENSIONAL ACCURACY OF SLIT (AT  $r=22.2\text{mm}$ )

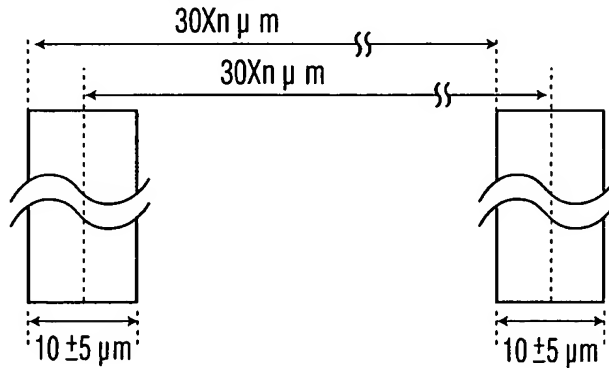


FIG. 36B

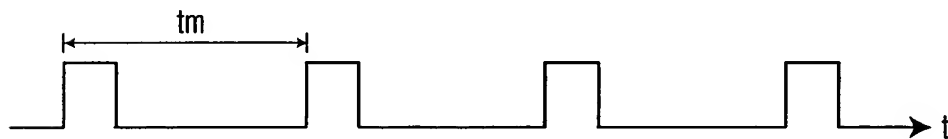


FIG. 36C



FIG. 36D

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(1) TIME SLOT

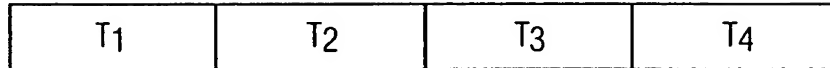


FIG. 37A

(2) CHANNEL BIT



FIG. 37B

(3) RECORDING PULSE

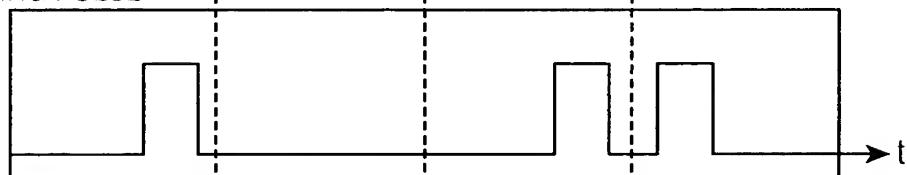


FIG. 37C

(4) EMITTING PULSE

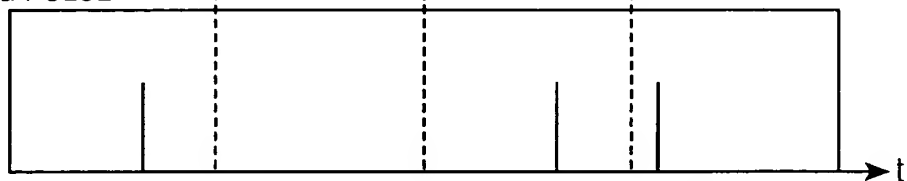


FIG. 37D



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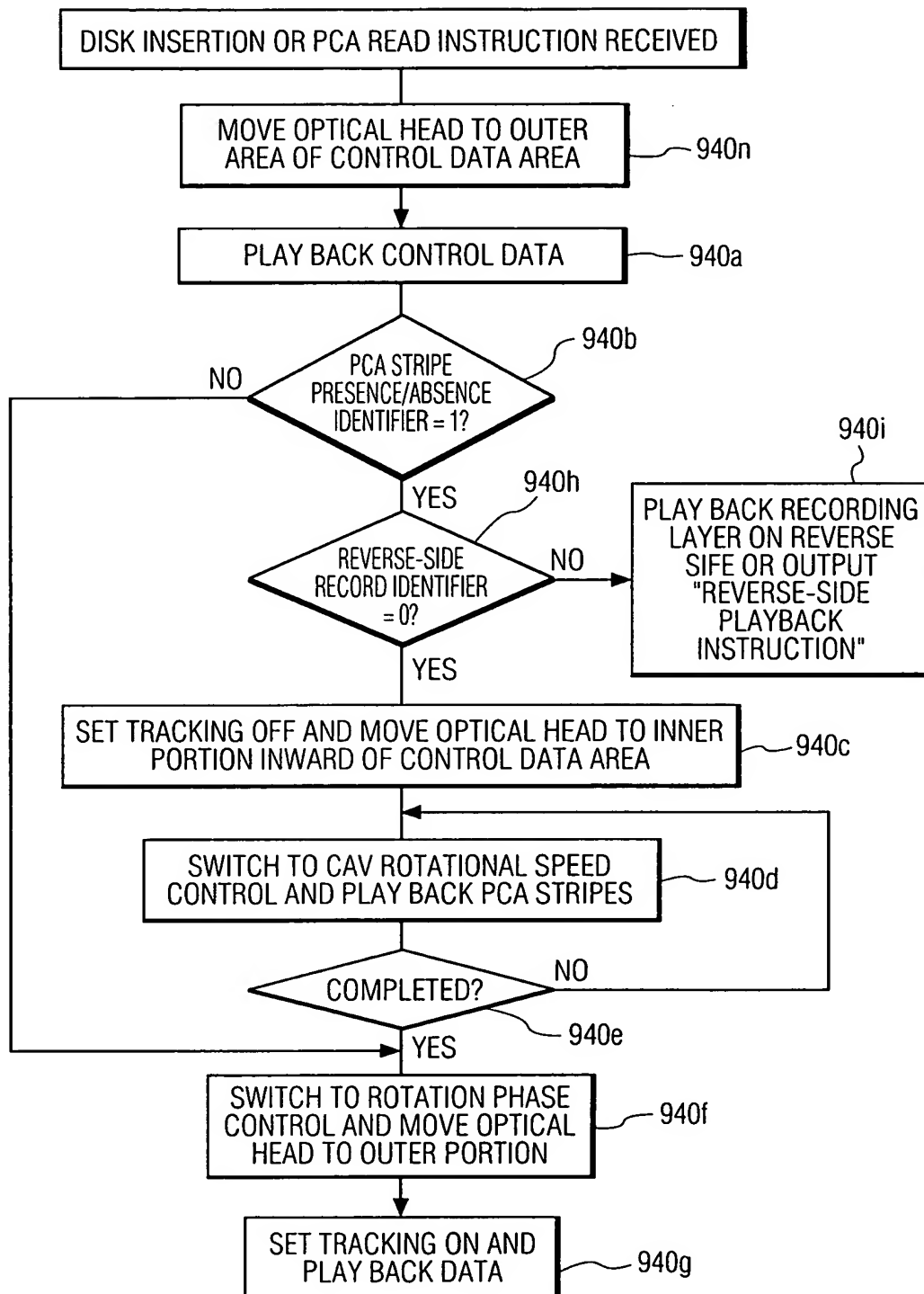
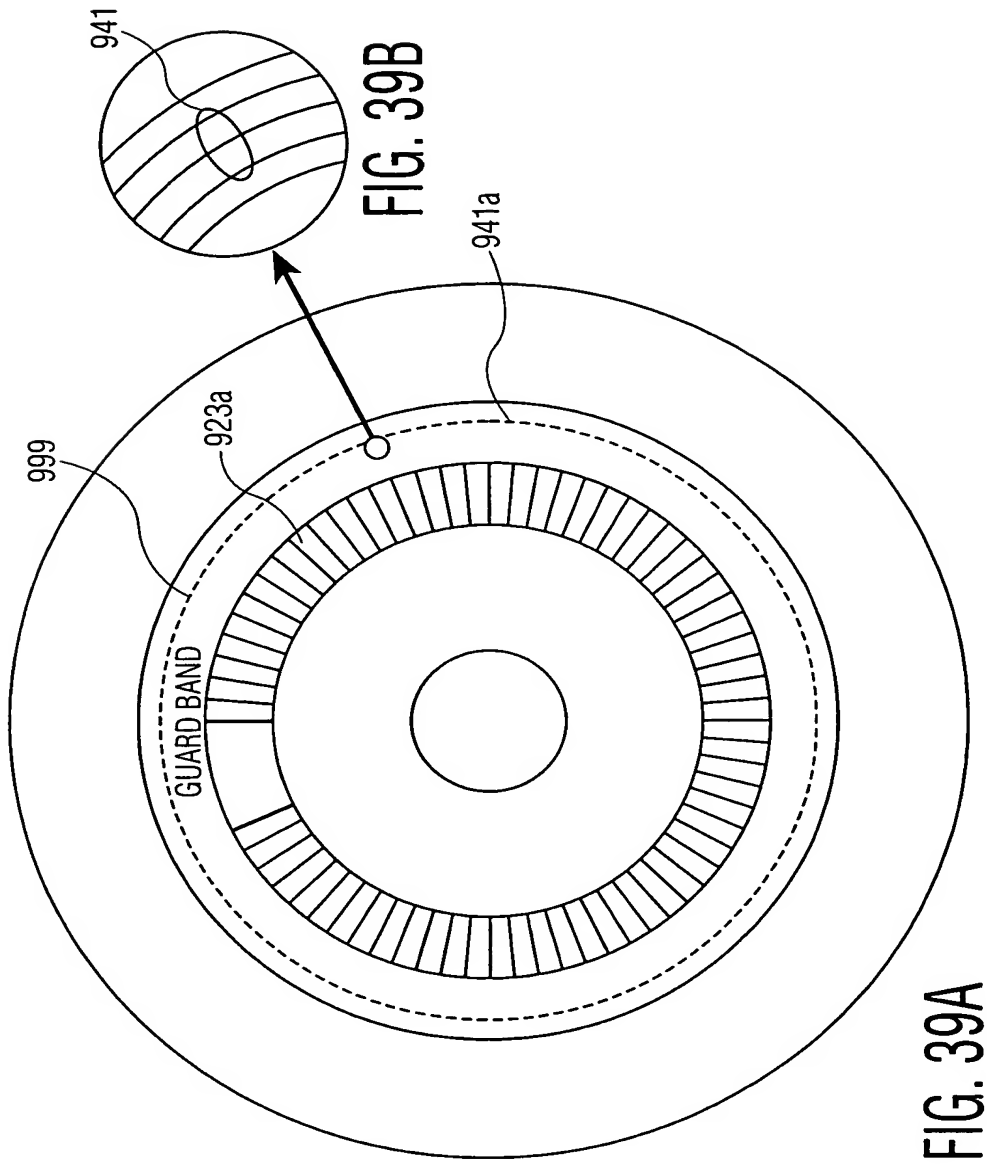
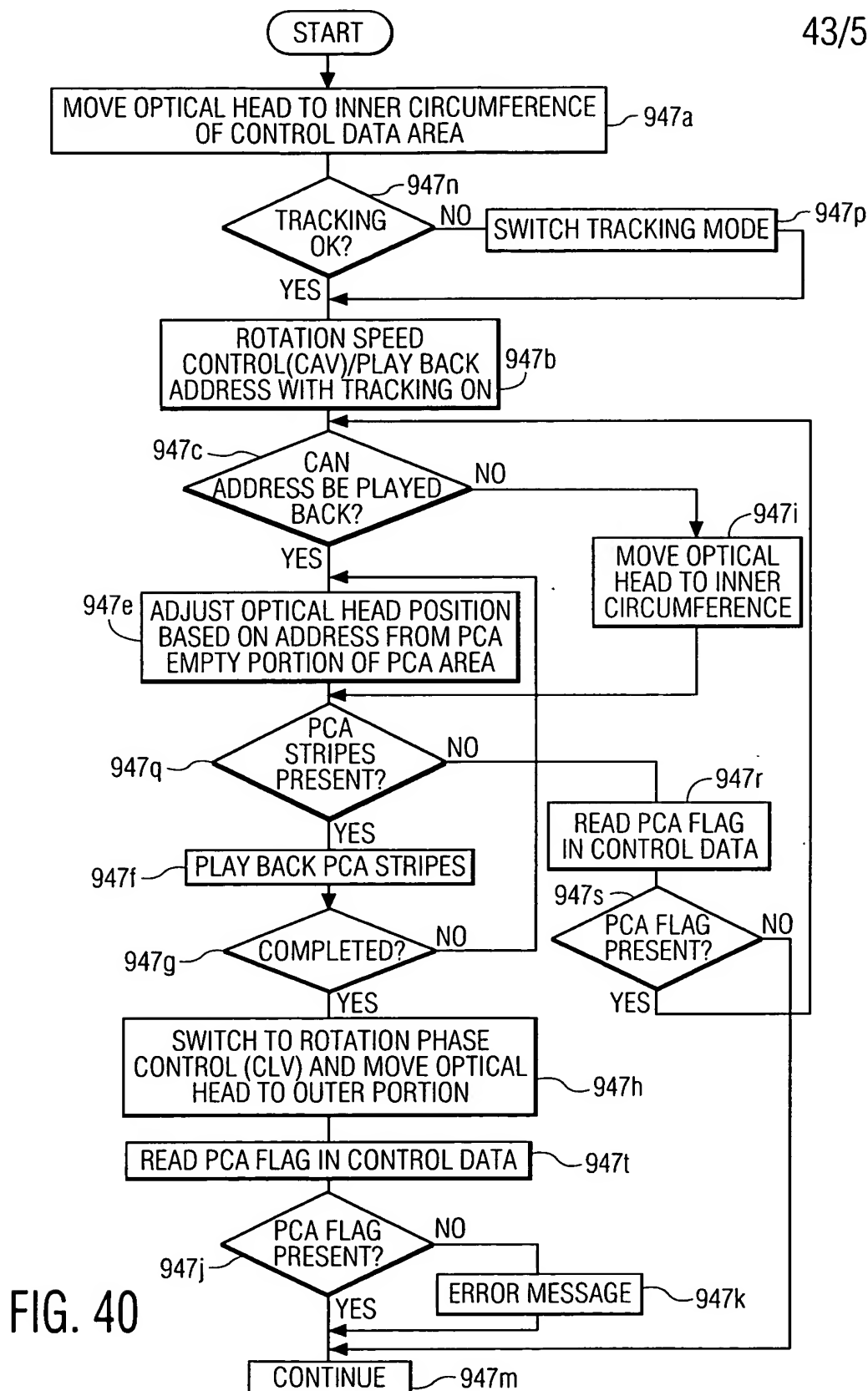


FIG. 38

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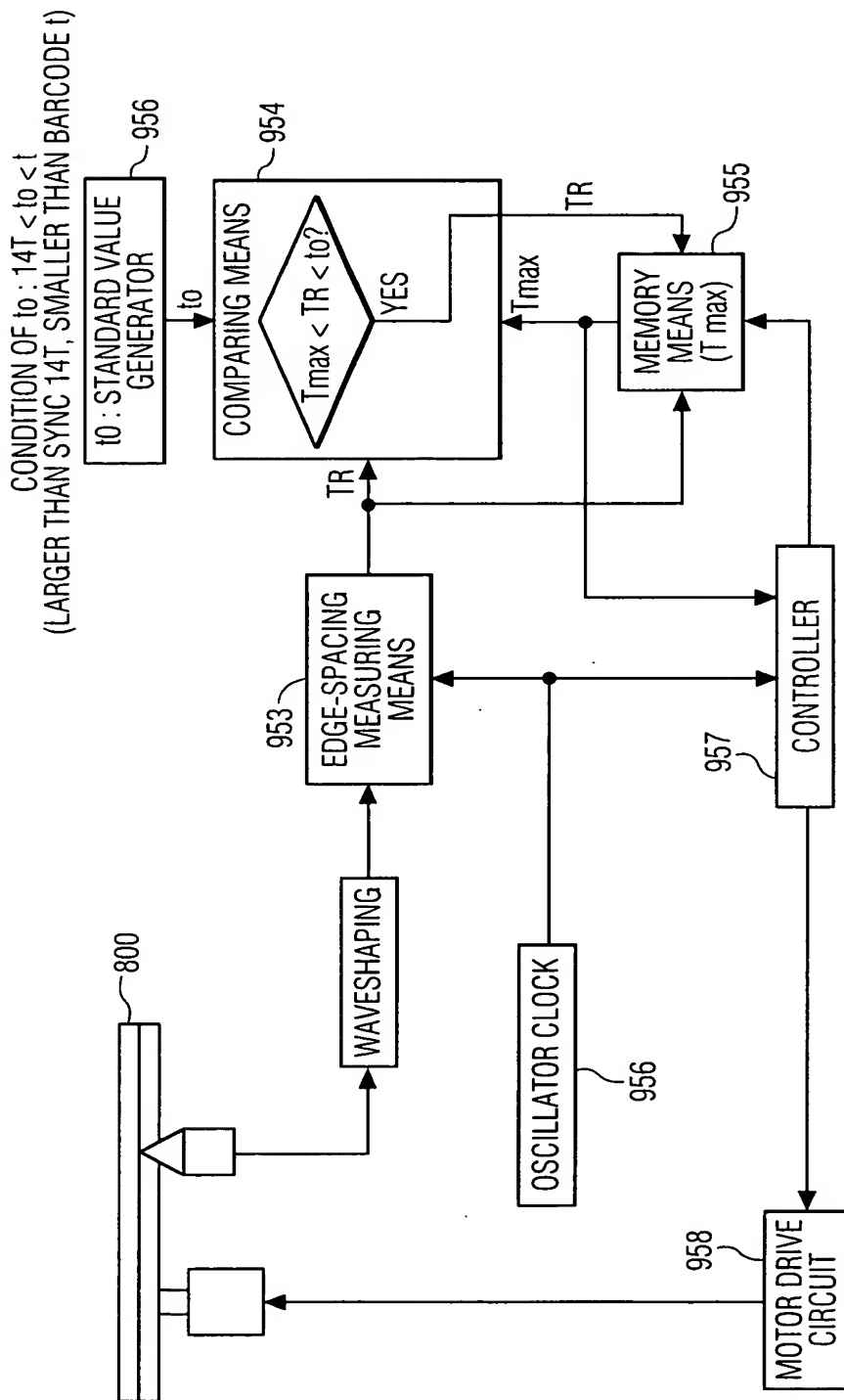


FIG. 41

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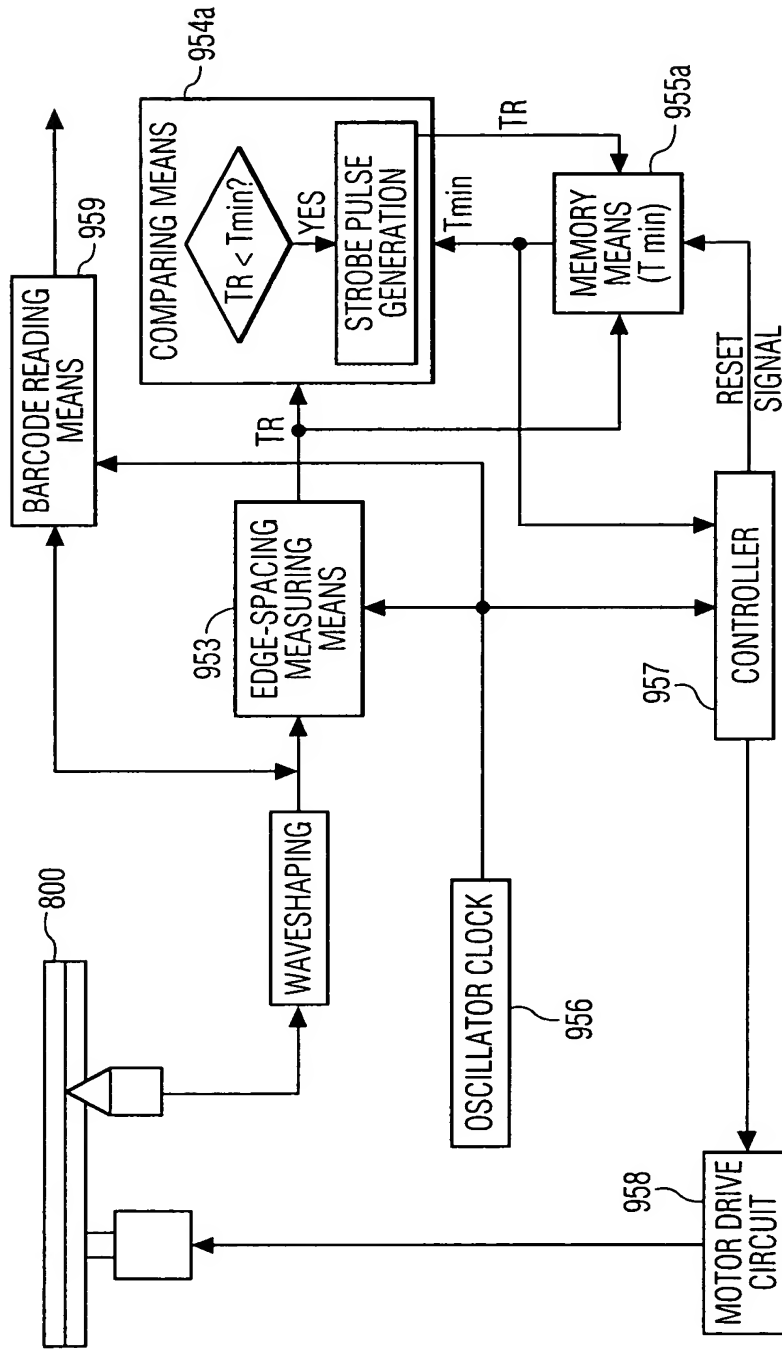


FIG. 42

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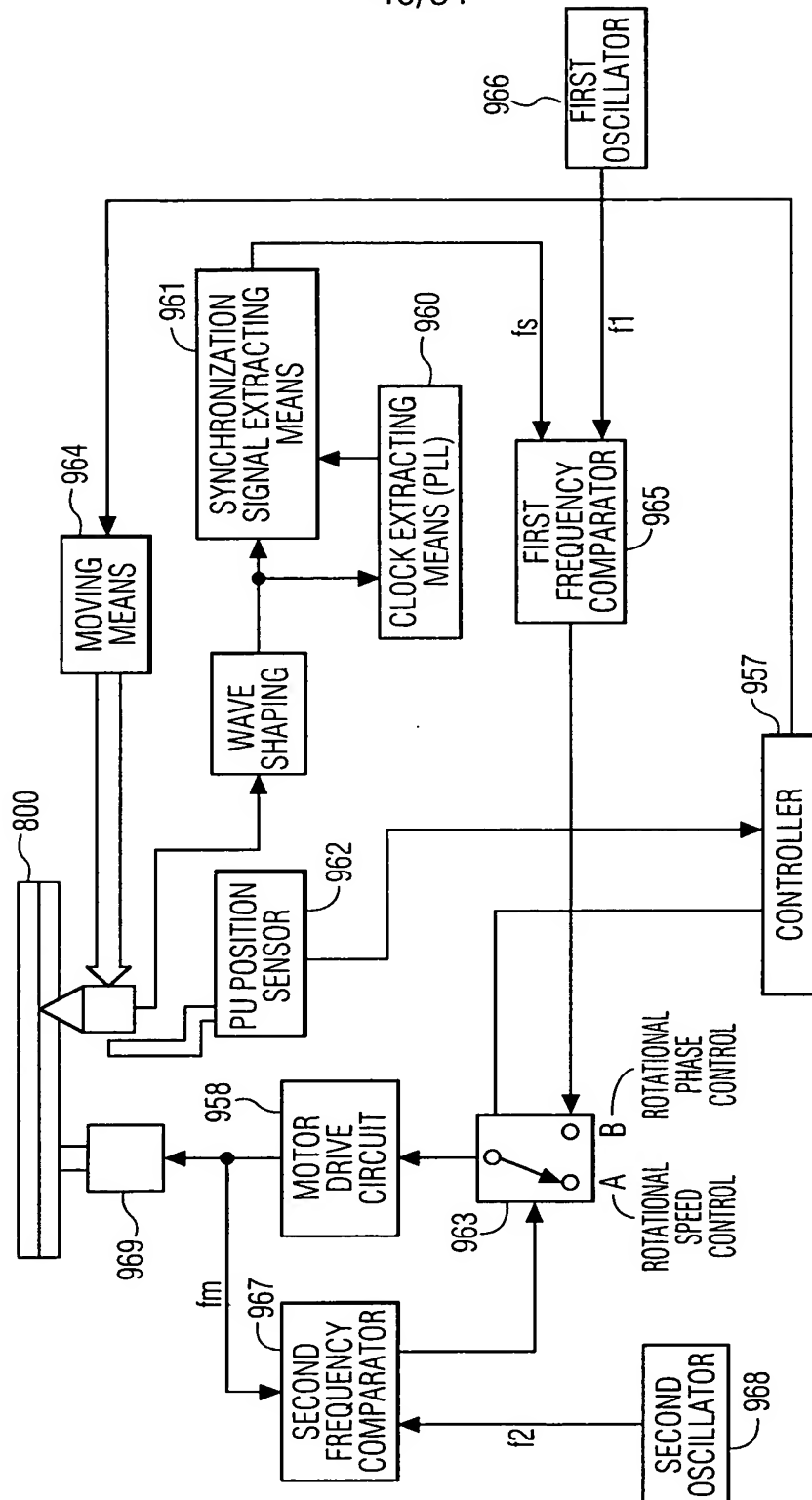


FIG. 43

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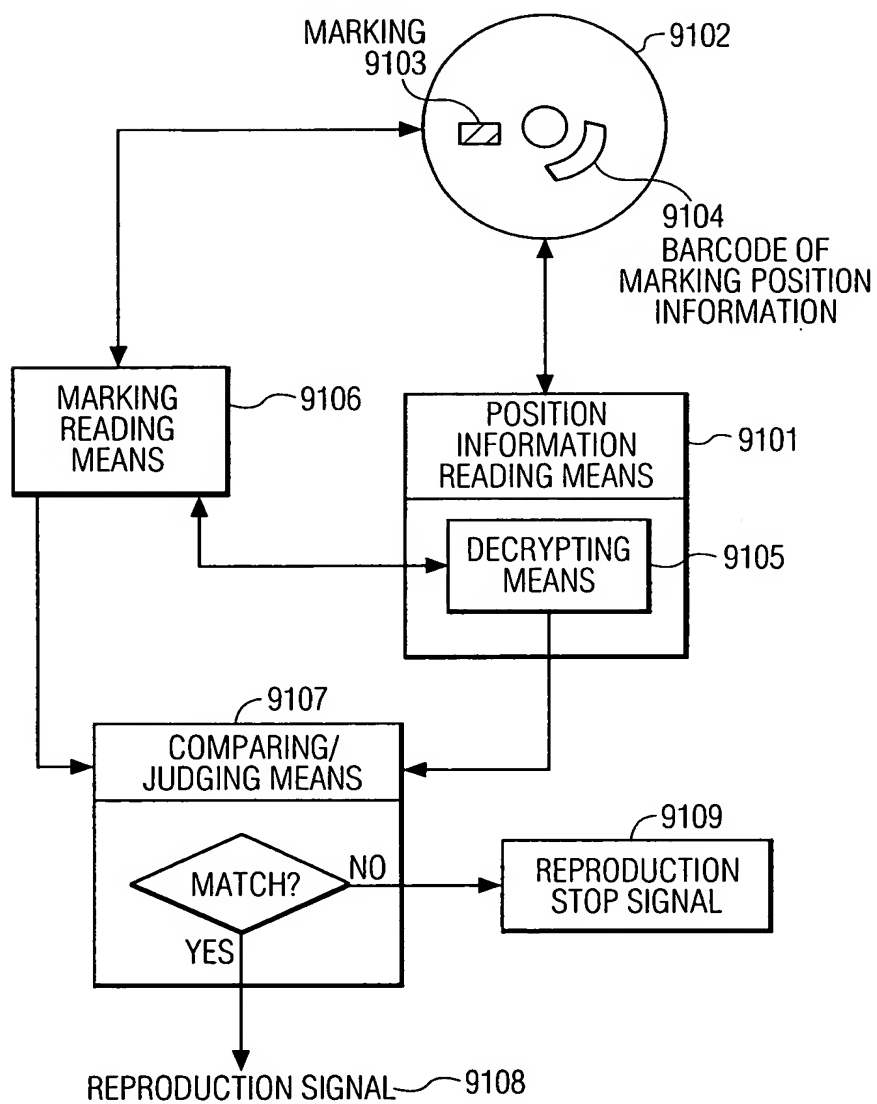


FIG. 44

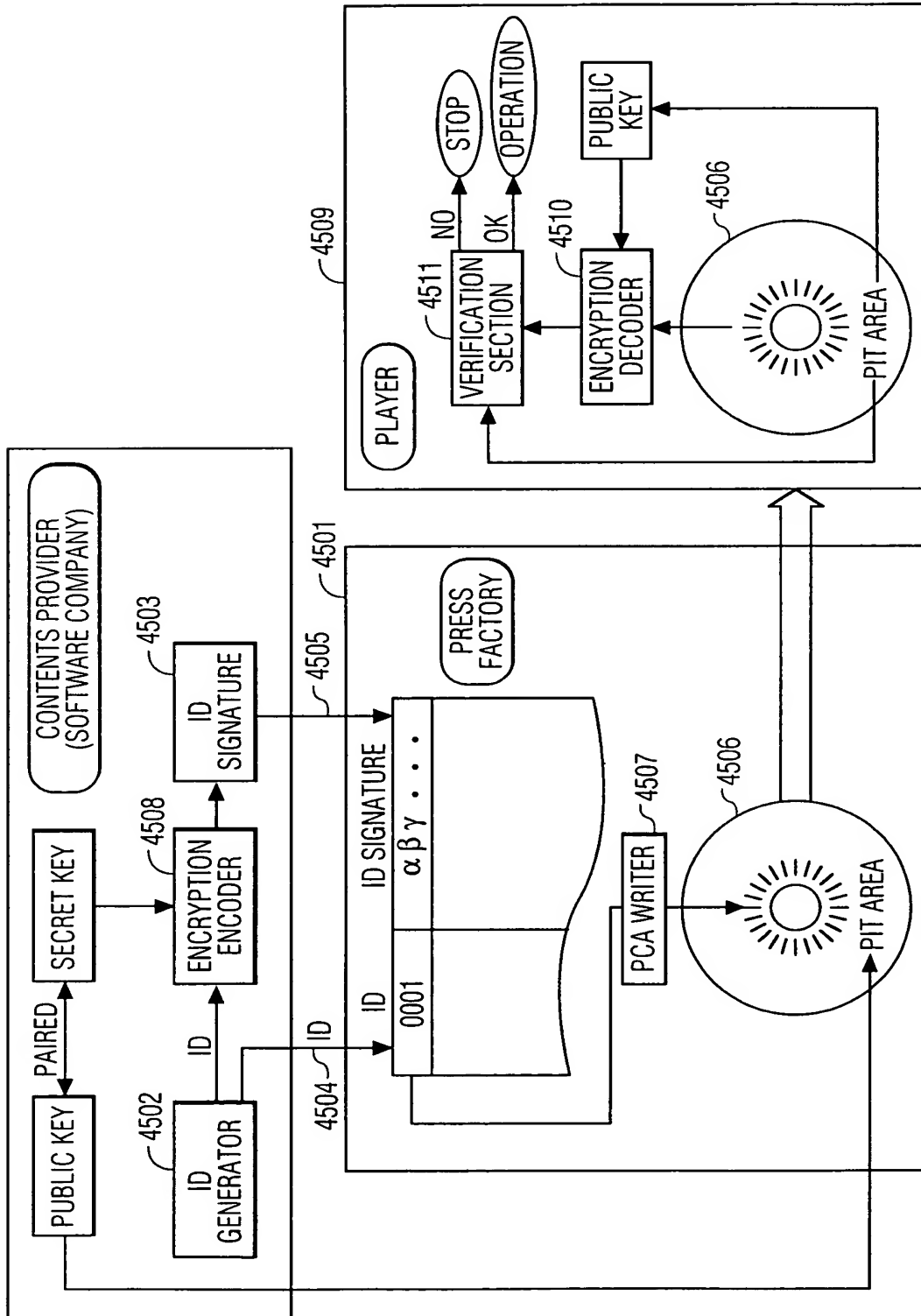


FIG. 45



FIG. 46

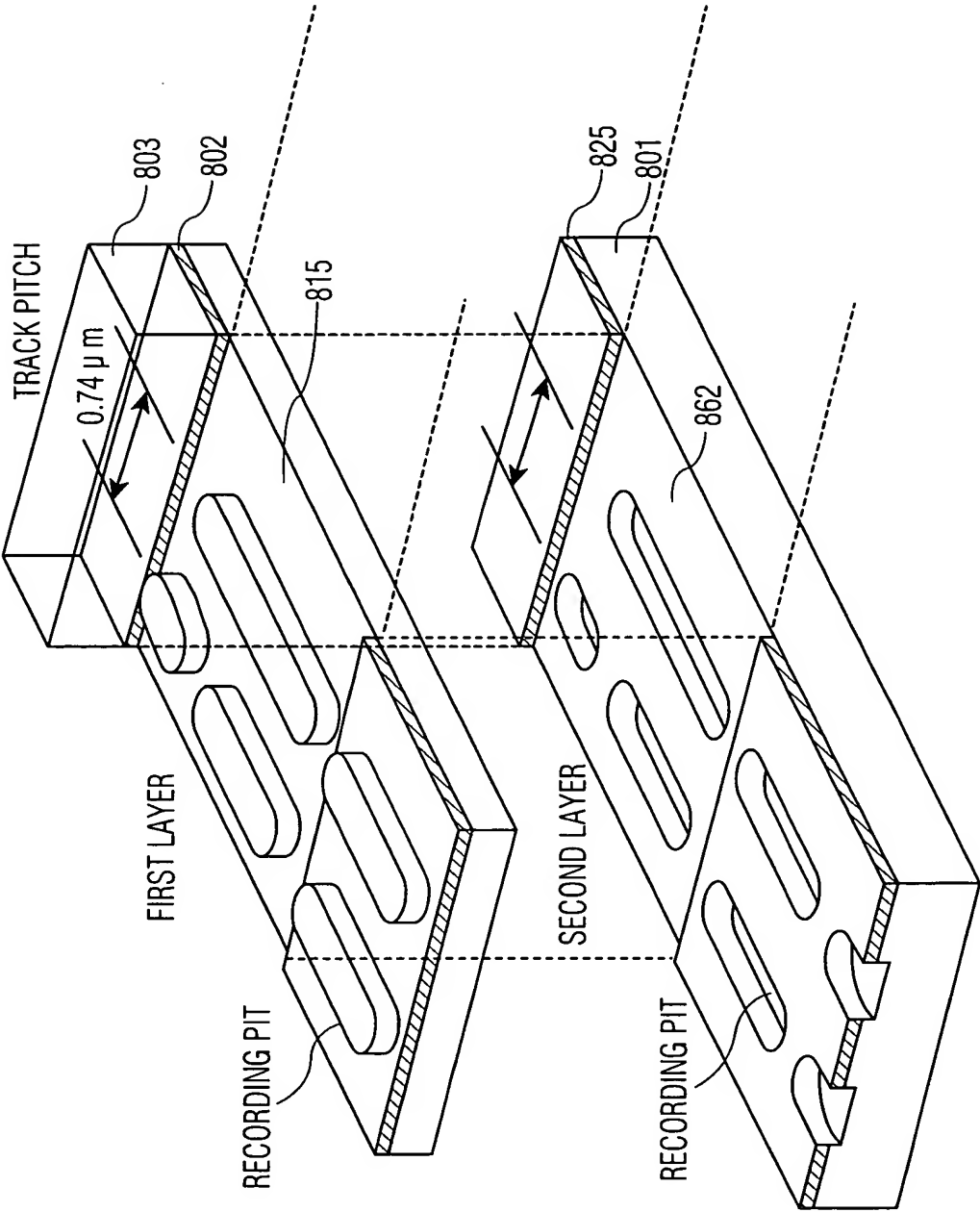


FIG. 47

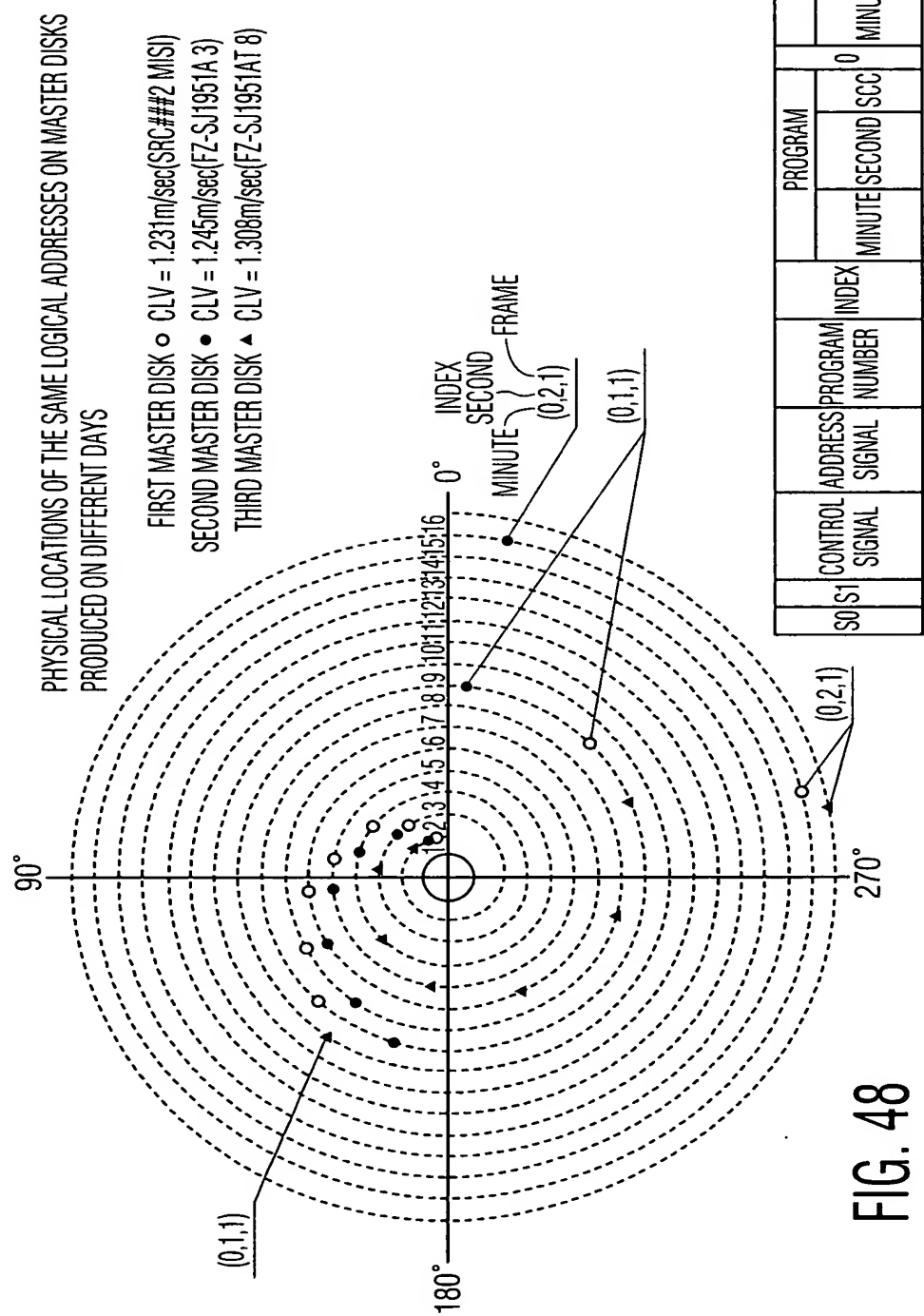


FIG. 48